5. DISASSEMBLY AND ASSEMBLY

ABOUT THIS CHAPTER

This chapter explains how to disassemble and assemble the various modules of the M20 system.

CONTENTS

5. DISASSEMBLY AND ASSEMBLY

****

BEFORE CARRYING OUT ANY OF THE FOLLOWING PROCEDURES, MAKE SURE THAT THE M20 IS SWITCHED OFF, THE AC CABLE IS REMOVED FROM THE SUPPLY AND THAT THE DISPLAY AND ANY PERIPHERALS ARE DISSCONNECTED FROM THE BASIC MODULE

****

5.1 BASIC MODULE

5.1.1 REMOVAL OF BASIC MODULE COVER

The Basic Module cover is maintained in place at the rear by two screws.

Tools required: Normal screwdriver.

1 - Loosen the two screws at the rear of the Basic Module cover (see Figure 5-1).

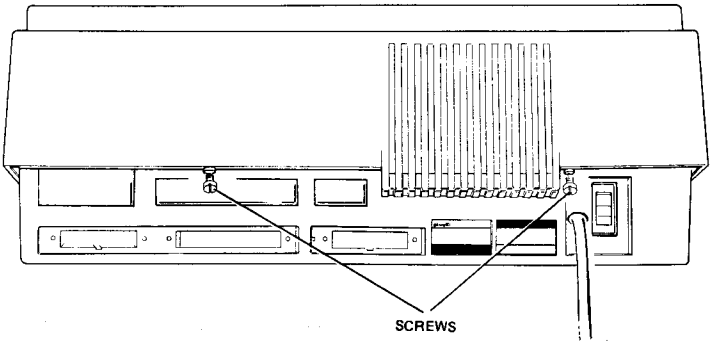


Fig. 5-1 Removal of Basic Module Cover

2 - Lift the rear of the cover.

3 - Remove the cover

4 - Remove the disk cover (see Figure 5-2).

To reinstall the Basic Module cover, perform the above operations in reverse order.

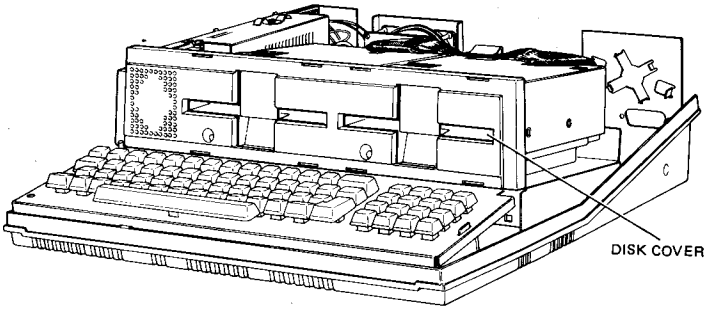


Fig. 5-2 Removal of Disk Cover

5.1.2 REMOVAL OF THE KEYBOARD

The Keyboard is maintained in place by the Basic Module cover and connected to the motherboard by means of a cable that connects to J11 on the mother board. This cable is hard wired to the keyboard.

Tools Required: Normal screwdriver.

1 - Remove the Basic Module cover and disk cover (see para 5.1.1).

2 - Remove the Keyboard from its two locating tabs (see Figure 5-3).

3 - Unplug the keyboard cable from connector J11 on the motherboard (see Figure 5-3).

To reinstall the keyboard, perform the above operations in reverse order.

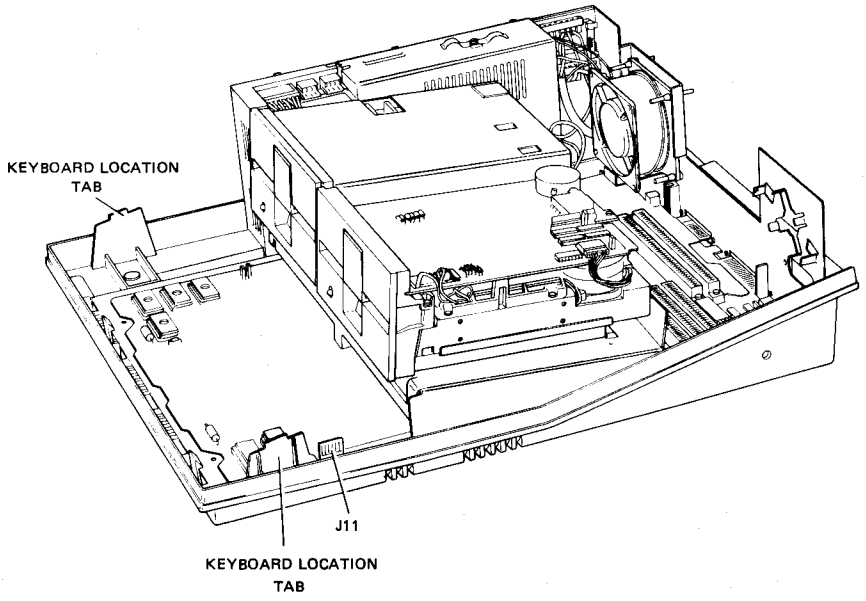


Fig. 5-3 Removal of Keyboard

5.1.3 REMOVAL OF THE DISKETTE DRIVE(S)

The M20 may have one or two diskette drives installed. The diskette drives are mounted on a plate that stradles the motherboard.

The procedure for removing a diskette drive from an M20 that has one disk drive installed is as follows:

Tools Required: Normal screwdriver

1 - Remove the Basic Module cover, disk cover (para 5.1.1) and keyboard (para 5.1.2)

2 - Remove the memory expansion boards, if installed (see Figure 5-4).

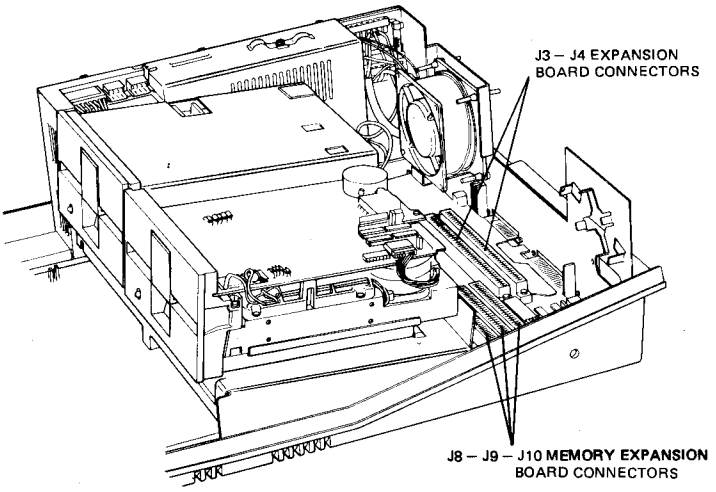


Fig. 5-4 Expansion Board Connector Positions

3 - Unplug the ribbon signal cable from connector J2 on the motherboard and from J1 on the diskette drive (see Figure 5-5).

4 - Unplug the power cable from J2 on the diskette drive (see Figure 5-5).

5 - Remove the Diskette Drive together with its mounting plate by first sliding the assembly slightly forward to disengage it from its locating tabs and then lifting it clear of the Basic Module.

6 - Remove the diskette drive from its mounting plate by removing the screw that fastens it to the front of the mounting plate and sliding it slightly forward to disengage it from its locating tabs.

To reinstall the diskette drive, perform the above operations in reverse order.

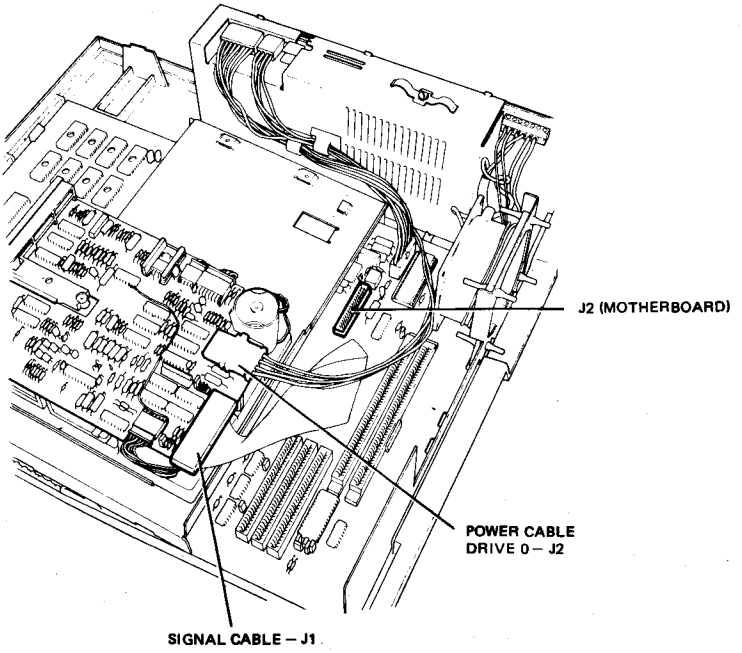


Fig. 5-5 Removal of One Diskette Drive

The procedure for removing the diskette drives form an M20 that has two diskette drives installed is as follows:

1 - Remove the Basic Module cover, disk cover (para 5.1.1) and keyboard (para 5.1.2).

2 - Remove the memory expansion boards, if installed (see Figure 5-4).

3 - Unplug the ribbon signal cable from connector J2 on the motherboard and from J1 on the two diskette drives (see Figure 5-6).

4 - Unplug the power cable from J2 on the two diskette drives (see Figure 5-6).

5 - Remove the Diskette Drives together with their mounting plate by first sliding the assembly slightly forward to disengage it from its locating tabs and then lifting it clear of the Basic Module.

6 - Remove the diskette drives from their mounting plate by removing the screws that fasten them to the front of the mounting plate and sliding them slightly forward to disengage them from their locating tabs.

To reinstall the Diskette Drives, perform the above operations in reverse order.

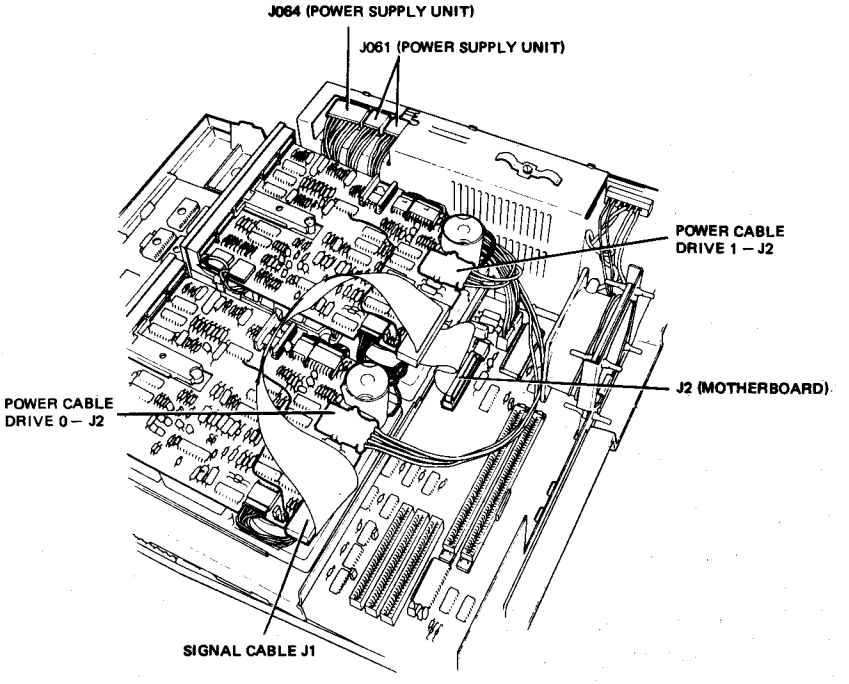


Fig. 5-6 Removal of Two Diskette Drives

5.1.4 REMOVAL OF THE POWER SUPPLY UNIT

The power supply is mounted on the left side of the Basic Module.

Tools Required: Normal screwdriver.

1 - Remove the Basic Module cover, disk cover (para 5.1.1) and keyboard (para 5.1.2).

2 - Unplug the cable that connects the power supply to the motherboard from connector J064 on the power supply unit (see Figure 5-6).

3 - Unplug the cable(s) that connect(s) the power supply to the diskette drive(s) from connector(s) J061 on the power supply unit (see Figure 5-6).

4 - Disconnect the power supply cable(s) and the wires that connect the power supply to the fan from the upper and lower terminal strips (see Figure 5-7).

5 - Disconnect the ground wire from the spade terminal on the motherboard (see Figure 5-7).

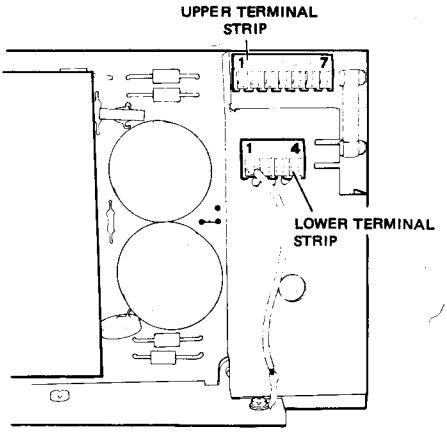
6 - Slide the power supply unit forward until it is released from its locating tabs on the base of the Basic Module and the power supply cable clamps are accessible.

7 - Loosen the two cable clamp screws.

8 - Remove the power supply cable through its entry hole at the rear of the Basic Module (see Figure 5-11).

9 - Remove the power supply unit from the Basic Module.

To reinstall the power supply unit, perform the above operations in reverse order.



	TERMINAL STRIP										
	UPPER							LOWER			
	1	2	3	4	5	6	7	1	2	3	4
POWER SUPPLY CABLE (L)					*						
POWER SUPPLY CABLE (N)				*							
POWER SUPPLY CABLE (GND)											*
COLOR DISPLAY POWER (L)							*				
COLOR DISPLAY POWER (N)			*								
COLOR DISPLAY POWER (GND)									*		
FAN POWER (L)		*									
FAN POWER (N)	*										
FAN POWER (GND)										*	
ON/OFF SWITCH LINE SIDE (L)					*						
ON/OFF SWITCH LINE SIDE (N)				*							
ON/OFF SWITCH M20 SIDE (L)						*					
ON/OFF SWITCH M20 SIDE (N)			*								

Fig. 5-7 Power Supply Unit Terminal Strips

5.1.5 REMOVAL OF THE MOTHERBOARD

The motherboard is mounted at the bottom of the Basic Module. Great care must be exercised in removing this board.

Tools Required: Normal screwdriver.

1 - Remove the Basic module cover, disk cover (para 5.1.1) and keyboard (para 5.1.2).

2 - Remove any memory expansion boards and option boards plugged into the motherboard (see Figure 5-4).

3 - Unplug the cable that connects the power supply to the motherboard from connector J1 on the motherboard (see Figure 5-8).

4 - Disconnect the ground wire from the spade terminal on the motherboard (see Figure 5-8).

4 - Remove the disk drive(s) and associated cables (para 5.1.3).

5 - Gently disengage the motherboard from the retaining clips at its front edge and the from the retaining lugs at its rear edge (see Figure 5-8).

6 - Remove the motherboard

To reinstall the motherboard, perform the above operations in reverse order.

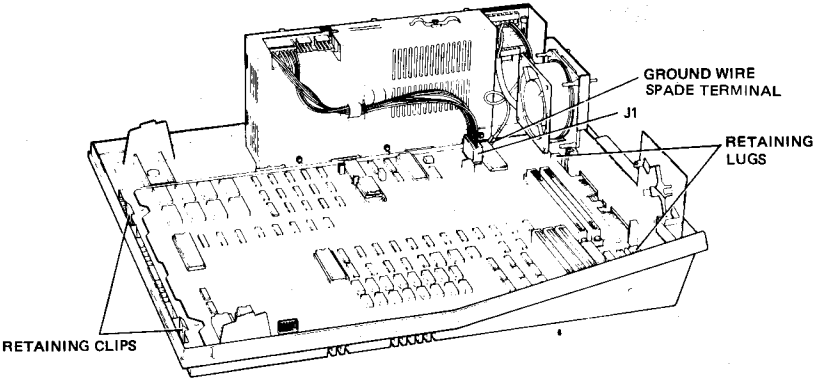


Fig. 5-8 Removal of the Motherboard

5.1.6 REPLACEMENT OF THE FUSE

The fuse is located at the rear of the power supply unit.

Tools Required: Normal screwdriver.

1 - Remove the Basic Module cover (para 5.1.1).

2 - Remove the fuse from its holder (see Figure 5-9).

To reinstall a fuse, perform the above operations in reverse order.

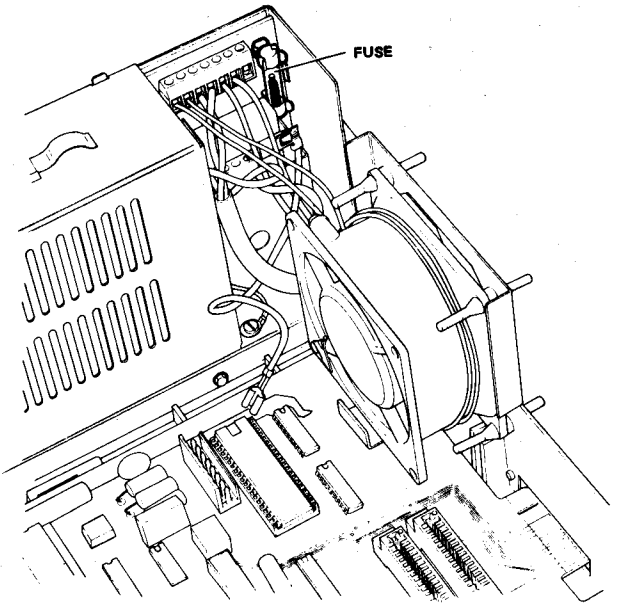


Fig. 5-9 Removal of the Fuse

5.1.7 REMOVAL OF THE FAN

The fan is mounted on a plate at the rear of the Basic Module by means of four rubber silent blocks.

Tools Required: Normal screwdriver and crosspoint screwdriver.

1 - Remove the Basic Module cover (see Figure 5.1.1).

2 - Disconnect the wires that connect the power supply to the fan from the upper and lower terminal strips (see Figure 5-7).

3 - Remove the rubber silent blocks that fasten the fan to the plate (see Figure 5-10).

4 - Remove the fan.

To reinstall the fan, perform the above operations in reverse order.

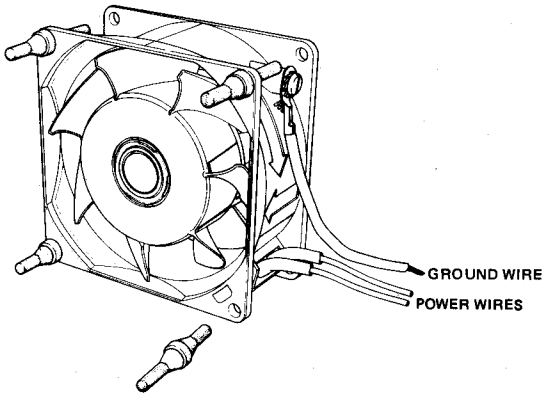


Fig. 5-10 Removal of the Fan

5.1.8 REMOVAL OF THE POWER SUPPLY CABLE

The mains power cable passes through an entry hole at the rear of the Basic Module.

Tools Required: Normal Screwdriver.

1 - Remove the Basic Module cover, disk cover (para 5.1.1) and keyboard (para 5.1.2).

2 - Disconnect the three wires of the power cable from the terminal strips (see Figure 5-7).

3 - Slide the power supply unit forward until the cable clamp screws are accessible.

4 - Loosen the two cable clamp screws.

5 - Remove the power supply cable through its entry hole at the rear of the Basic Module (see Figure 5-11).

To reinstall the power supply cable, perform the above operations in reverse order.

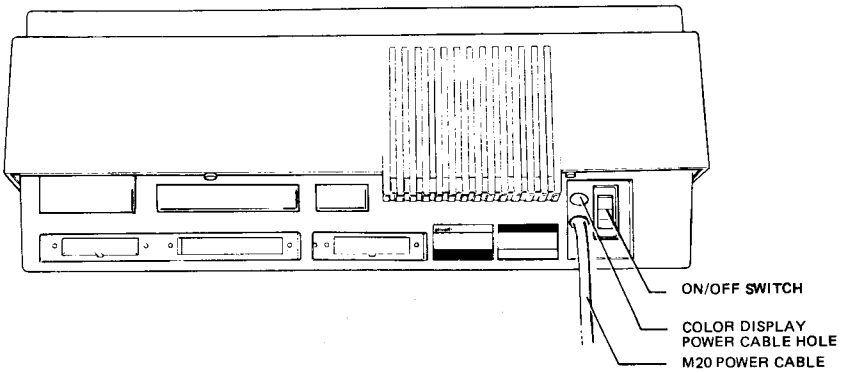


Fig. 5-11 Removal of the Power Supply Cable & ON/OFF Switch

5.1.9 REMOVAL OF THE ON/OFF SWITCH

The ON/OFF switch is located at the rear of the Basic Module and is housed in the power supply unit.

Tools Required: Normal screwdriver.

1 - Remove the Basic Module cover (para 5.1.1).

2 - Disconnect the four wires of the ON/OFF switch from the upper terminal strip of the power supply unit (see Figure 5-7).

3 - Remove the ON/OFF switch.

To reinstall the ON/OFF switch, perform the above operations in reverse order.

5.2 CRT DISPLAY

5.2.1 REMOVAL OF CRT DISPLAY COVER

Tools Required: Normal screwdriver and Allen Key

1 - Loosen the two screws located in the handle recess at the top of the CRT Display cover.

2 - Loosen the four Allen screws at the bottom of the CRT Display cover (see Figure 5-12).

3 - Gently separate the cover and remove it from the CRT Display.

To reinstall the CRT display cover, perform the above operations in reverse order.

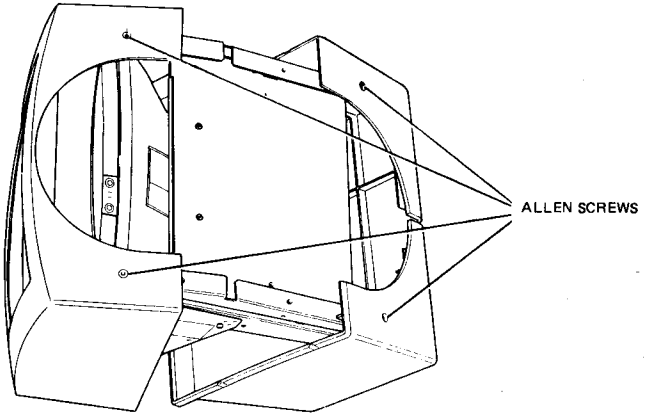


Fig. 5-12 Removal of the CRT Display Cover

6. LSI CHARACTERISTICS

ABOUT THIS CHAPTER

This chapter lists all the characteristics of the Large Scale Integrated circuits found on the M20 motherboard.

CONTENTS

6. LSI CHARACTERISTICS

6.1 GENERAL

The following characteristics are included for reference purposes only. For detailed information, refer to component manufacturer's data sheets.

6.2 Z8001 - CENTRAL PROCESSOR UNIT

ABSOLUTE MAXIMUM RATINGS

Operating Temperature .. .. 0 to 70 degC
Storage Temperature .. .. -65 to +150 degC
Voltage On Any Pin WRT Ground .. .. -0.3V to +7V

STANDARD TEST CONDITIONS

The characteristics listed below apply for the following test conditions unless otherwise noted. All Voltages are referenced to GND. Positive current flows into referenced pin.

Standard conditions are as follows:

+4.75V < VCC < +5.25V
GND = 0V
0 degC < TA < +70 degC

D.C. CHARACTERISTICS

SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITIONS
VCH	Clock Input High Voltage	VCC-.4	VCC+.3	V	Driven by Ext Clk Gen
VCL	Clock Input Low Voltage	-0.3	0.45	V	Driven by Ext Clk Gen
VIH	Input High Voltage	2.0	VCC+.3	V	
VIHRESET	High Voltage on Reset Pin	2.4	VCC-.3	V	
VIL	Input Low Voltage	-0.3	0.8	V	
VOH	Output High Voltage	2.4		V	IOH = -250 uA
VOL	Output Low Voltage		0.4	V	IOL = 2.0 uA
IIL	Input Leakage		±10	uA	0.4 < VIN < + 2.4V
IILSEGT	Input Leakage on SEGT Pin	-100	100	uA	
IOL	Output Leakage		±10	uA	0.4 < VIN < + 2.4V
ICC	VCC Supply Current		300	mA	

A.C. CHARACTERISTICS

No	SYMBOL	PARAMETER	MIN (ns)	MAX (ns)
1	TcC	Clock Cycle Time	250	2000
2	TwCh	Clock Width High	105	2000
3	TwCl	Clock Width Low	105	2000
4	TfC	Clock Fall Time		20
5	TrC	Clock Rise Time		20
6	TdC(SNv)	Clock ↓ to Segment Number Valid (50 pF load)		130
7	TdC(SNn)	Clock ↓ to Segmant Number Not Valid	20	
8	TdC(Bz)	Clock ↓ to Bus Float		65
9	TdC(A)	Clock ↓ to Address Valid		100
10	TdC(Az)	Clock ↓ to Address Float		65
11	TdA(DI)	Address Valid to Data In Required Valid		455
12	TsDI(C)	Data In to Clock ↑ Set Up Time	50	
13	TdDS(A)	*DS ↓ to Address Active	80	
14	TdC(DO)	Clock ↓ to Data Out Valid		100
15	ThDI(DS)	Data In to *DS ↑ Hold Time	0	
16	TdDO(DS)	Data Out Valid to *DS ↑ Delay	295	
17	TdAMR	Address Valid to MREQ ↓ Delay	55	
18	TdC(MR)	Clock ↓ to MREQ ↓ Delay		80
19	TwMRh	MREQ Width High	210	
20	TdMR(A)	MREQ ↑ to Address Not Active	70	
21	TdDO(DSW)	Data Out Valid to *DS ↑ (Write) Delay	55	
22	TdMR(DI)	MREQ ↑ to Data In Required Valid		350
23	TdC(MR)	Clock ↑ MREQ ↓ Delay		80
24	TdC(ASf)	Clock ↓ to *AS ↓ Delay		80
25	TdA(AS)	Address Vaild to *AS ↓ Delay	55	
26	TdC(ASr)	Clock ↑ to *AS ↓ Delay		90
27	TdAS(DI)	*AS ↓ to Data In Required Valid		340
28	TdDS(AS)	*DS ↓ to *AS ↑ Delay	70	
29	TwAS	*AS Width Low	85	
30	TdAS(A)	*AS ↑ to Address Not Active Delay	60	
31	TdAz(DSR)	Address Float to *DS (Read) ↓ Delay	0	
32	TdAS(DSR)	*AS ↓ to *DS (Read) ↓ Delay	70	
33	TdDSR(DI)	*DS (Read) ↓ to Data In Required Valid		185
34	TdC(DSr)	Clock ↑ to *DS ↓ Delay		70
35	TdDS(DO)	*DS ↑ to Data Out and STATUS Not Valid	75	
36	TdA(DSR)	Address Valid to *DS (Read) ↓ Delay	180	
37	TdC(DSR)	Clock ↑ to *DS (Read) ↓ Delay		120
38	TwDSR	*DS (Read) Width Low	275	
39	TdC(DSW)	Clock ↑ to *DS (Write) ↓ Delay		95
40	TwDSW	*DS (Write) Width Low	185	
41	TdDSI(DI)	*DS (Input) ↑ to Data In Required Valid		320
42	TdC(DSf)	Clock ↑ to *DS (I/O) ↑ Delay		120
43	TwDS	*DS (I/O) Width Low	410	
44	TdAS(DSA)	*AS ↑ to *DS (Acknowledge) ↑ Delay	1065	
45	TdC(DSA)	Clock ↓ to *DS (Acknowledge) ↑ Delay		120
46	TdDSA(DI)	*DS (Acknowledge) ↑ to Data In Required Delay		435
47	TdC(S)	Clock ↓ to Status Valid Delay		110
48	TdS(AS)	Status Valid to *AS ↓ Delay	50	
49	TsR(C)	*RESET to Clock ↓ Set Up Time	180	
50	ThR(C)	*RESET to Clock ↓ Hold Time	0	
51	TwNMI	*NMI Width Low	100	
52	TsNMI(C)	*NMI to Clock ↓ Set Up Time	140	
53	TsVI(C)	*VI,NVI to Clock ↓ Set Up Time	110	
54	ThVI(C)	*VI,NVI to Clock ↓ Hold Time	0	
55	TsSGT(C)	*SEGT to Clock ↓ Set Up Time	70	
56	ThSGT(C)	*SEGT to Clock ↓ Hold Time	0	
57	TsMI(C)	*MI to Clock ↓ Set Up Time	180	
58	ThMI(C)	*MI to Clock ↓ Hold Time	0	
59	TdC(MO)	Clock ↓ to MO Delay		120
60	TsSTP(C)	*STOP to Clock ↓ Set Up Time	140	

A.C. CHARACTERISTICS (Cont.)

No	SYMBOL	PARAMETER	MIN (ns)	MAX (ns)
61	ThSTP(C)	*STOP to Clock ↑ Hold Time	0	
62	TsWT(C)	*WAIT to Clock ↑ Set Up Time	50	
63	ThWT(C)	*WAIT to Clock ↑ Hold Time	10	
64	TsBRQ(C)	*BUSREQ to Clock ↓ Set Up Time	90	
65	ThBRQ(C)	*BUSREQ to Clock ↓ Hold Time	10	
66	TdC(BAKr)	Clock ↓ to *BUSACK ↓ Delay		100
67	TdC(BAKf)	Clock ↓ to *BUSACK ↑ Delay		100

CLOCK CYCLE TIME DEPENDENT CHARACTERISTICS

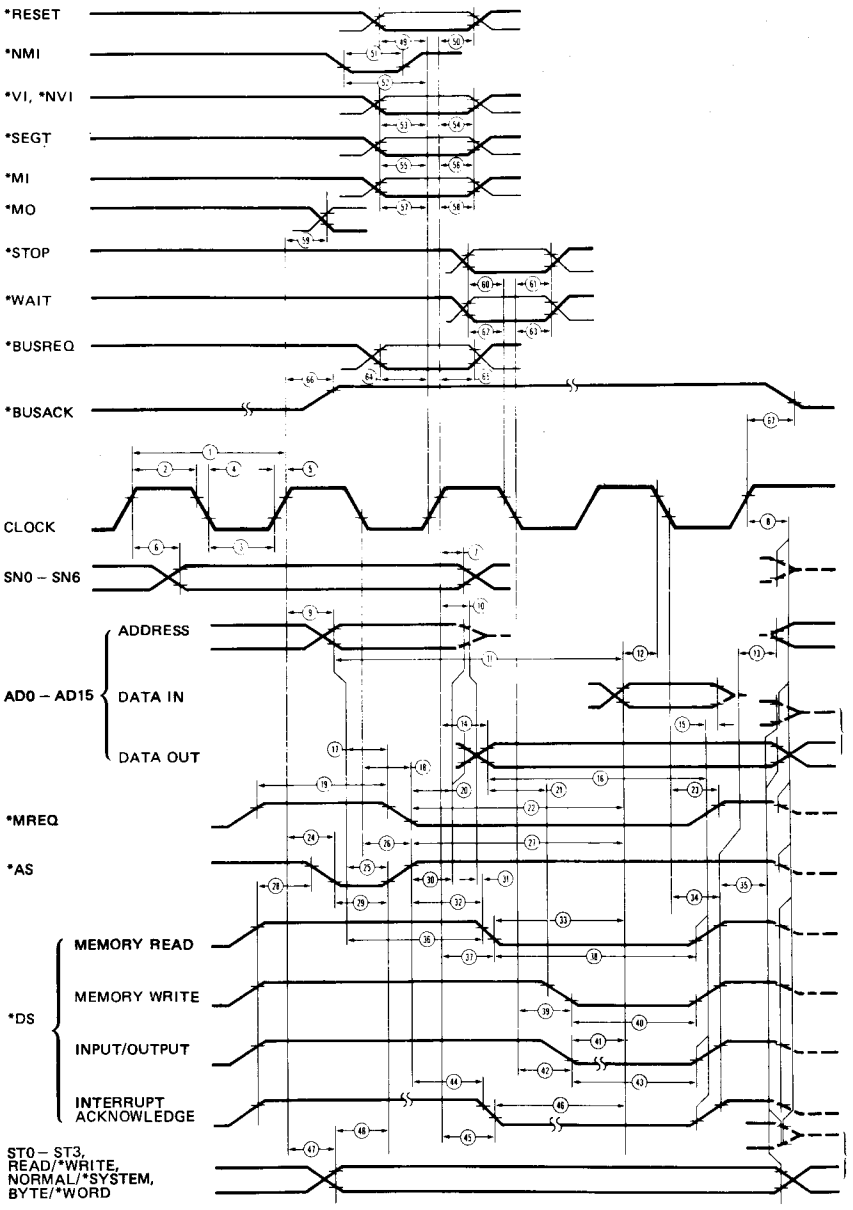
No	SYMBOL	EQUATION
11	TdA(DI)	2TcC + TwCh -150 ns
13	TdDS(A)	TwCl - 25 ns
16	TdDO(DS)	TcC + TwCh - 60 ns
17	TdAMR	TwCh - 50 ns
19	TwMRh	TcC - 40 ns
20	TdMR(A)	TwCl - 35 ns
21	TdDO(DSW)	TwCh - 50 ns
22	TdMR(DI)	2TcC - 150 ns
25	TdA(AS)	TwCh - 50 ns
27	TdAS(DI)	2TcC - 160 ns
28	TdDS(AS)	TwCl -35 ns
29	TwAS	TwCh -20 ns
30	TdAS(A)	TwCl - 45 ns
32	TdAS(DSR)	TwCl - 35 ns
33	TdDSR(DI)	TcC + TwCh - 170 ns
35	TdDS(DO)	TwCl - 30 ns
36	TdA(DSR)	TcC - 70 ns
38	TwDSR	TcC + TwCh - 80 ns
40	TwDSW	TcC - 65 ns
41	TdDSI(DI)	2TcC - 180 ns
43	TwDS	2TcC - 90 ns
44	TdAS(DSA)	4TcC + TwCl - 40 ns
46	TdDSA(DI)	2TcC + TwCh - 170 ns
48	TdS(AS)	TwCh - 55 ns

The following diagram does not show actual timing sequences. Reference should only be made to this diagram for detailed timing relationships of individual edges.

Timing measurements are made at:

	High	Low
Clock	4.0V	0.8V
Output	2.0V	0.8V
Input	2.0V	0.8V
Float	V	±0.5V

COMPOSITE A.C. TIMING DIAGRAM



6.3 8251A - PROGRAMMABLE COMMUNICATION INTERFACE

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias .. .. 0 to 70 degC
Storage Temperature .. .. -65 to +150 degC
Voltage On Any Pin WRT Ground .. .. -0.5V to +7V
Power Dissipation .. .. 1 W

D.C. CHARACTERISTICS (TA = 0 to 70 degC, VCC = +5V ±5%, GND = 0V)

SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITIONS
VIL	Input Low Voltage	-0.5	0.8	V	
VIH	Input High Voltage	2.0	VCC	V	
VOL	Output Low Voltage		0.45	V	IOL = 2.2mA
VOH	Output High Voltage	2.4		V	IOH = -400 uA
ICC	Power Supply Current		100	mA	All outputs = High
IIL	Input Load Current		±10	uA	VIN = VCC to .45V
IOFL	Output Float Leakage		±10	uA	VOUT = VCC to .45V

CAPACITANCE (TA = 25 degC, VCC = GND = 0V)

SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITION
CIN	Input Capacitance		10	pF	fc = 1 MHz
CI/O	I/O Capacitance		20	pF	unmeasured pins GND

A.C. CHARACTERISTICS (TA = 0 to 70 degC, VCC = +5V ±5%, GND = 0V)

Bus Parameters (Note 1)

READ

SYMBOL	PARAMETER	MIN	MAX	UNIT
tAR	Address Stable Before *READ (*CS,C/*D) 2	0		ns
tRA	Address Hold Time for *READ (*CS,C/*D) 2	0		ns
tRR	*READ Pulse Width	250		ns
tRD	Data Valid From *READ (CL = 150 pF) 3		200	ns
tDF	*READ to Data Floating	10	100	ns

WRITE

SYMBOL	PARAMETER	MIN	MAX	UNIT
tAW	Address Stable Before *WRITE	0		ns
tWA	Address Hold Time for *WRITE	0		ns
tWW	*WRITE Pulse Width	250		ns
tDW	Data Set Up Time for *WRITE	150		ns
tWD	Data Hold Time for *WRITE	20		ns
tRV	Recovery Tome Between WRITEs (4)	6		tCY

OTHER TIMINGS

SYMBOL	PARAMETER	MIN	MAX	UNIT
tCY	Clock Period (5) (6)	320	1350	ns
to	Clock High Pulse Width	120	tCY-90	ns
to	Clock Low Pulse Width	90		ns
tR, tF	Clock Rise and Fall Time		20	ns
tDTx	TxD Delay from Falling Edge of *TxC		1	us
tTX	Transmitter Input Clock Frequency			
	1 x Baud Rate	dc	64	KHz
	16 x Baud Rate	dc	310	KHz
	64 x Baud Rate	dc	615	KHz
tTPW	Transmitter Input Clock Pulse Width			
	1 x Baud Rate	12		tCY
	16 x and 64 x Baud Rate	1		tCY
tTPD	Transmitter Input Clock Pulse Delay			
	1 x Baud Rate	15		tCY
	16 x and 64 x Baud Rate	3		tCY
tRX	Receiver Input Clock Frequency			
	1 x Baud Rate	dc	64	KHz
	16 x Baud Rate	dc	310	KHz
	64 x Baud Rate	dc	615	KHz
tRPW	Receiver Input Clock Pulse Width			
	1 x Baud Rate	12		tCY
	16 x and 64 x Baud Rate	1		tCY
tRPD	Receiver Input Clock Pulse Delay			
	1 x Baud Rate	15		tCY
	16 x and 64 x Baud Rate	3		tCY
tTxRDY	TxRDY Delay from Centre of Last Bit (7)		8	tCY
tTxRDY CLR	TxRDY ↓ from Leading Edge of *WR (7)		400	us
tRxRDY	RxRDY Delay from Centre of Last Bit (7)		26	tCY
tRxRDY CLR	RxRDY ↓ from Leading Edge of *RD (7)		400	ns

tIS	Internal SYNDET Delay from Rising Edge of *RxC (7)		26	tCY
tES	External SYNDET Set Up Time After Rising Edge of *RxC (7)	18		tCY
tTxEMPTY	TxEMPTY Delay from Centre of Last Bit(7)	20		tCY
tWC	Control Delay from Rising Edge of WRITE (TxE,*DTR,*RTS) (7)	8		tCY
tCR	Control to READ set Up Time (*DSR,*CTS)7	20		tCY

1. AC timings measured VOH = 2.0VOL = 2.0, VOL = 0.8, and with CL = 150 pF.
2. CS and C/D are considered as addresses.
3. Assumes that address is valid before RD
4. This recovery time is for Mode initialization only. Write Data is allowed only when TxRDY = 1. Recovery time between Writes for Asynchronous Mode is 8 tCY and for Synchronous Mode is 16 tCY.
5. The TxC and RxC frequencies have limitations with respect to CLK.
6. Reset pulse width = 6 tCY minimum. System clock must be running during reset.
7. Status update can have a maximum delay of 28 clock periods from the event affecting the status.

6.4 8253-5 - PROGRAMMABLE INTERVAL TIMER

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias .. .. 0 to 70 degC
Storage Temperature .. .. -65 to +150 degC
Voltage On Any Pin WRT Ground .. .. -0.5V to +7V
Power Dissipation .. .. 1 W

D.C. CHARACTERISTICS (TA = 0 to 70 degC, VCC = +5V ±10%)

SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITIONS
VIL	Input Low Voltage	-0.5	0.8	V	
VIH	Input High Voltage	2.2	VCC+.5V	V	
VOL	Output Low Voltage		0.45	V	IOL = 2.2 mA
VOH	Output High Voltage	2.4		V	IOH = -400 uA
ICC	Power Supply Current		140	mA	
IIL	Input Load Current		±10	uA	VIN = VCC to 0V
IOFL	Output Float Leakage		±10	uA	VOUT = VCC to .45V

CAPACITANCE (TA = 25 degC, VCC = GND = 0V)

SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITION
CIN	Input Capacitance		10	pF	fc = 1 MHz
CI/O	I/O Capacitance		20	pF	unmeasured pins GND

A.C. CHARACTERISTICS (TA = 0 to 70 degC, VCC = +5V ±5%, GND = 0V)

Bus Parameters (Note 2)

READ

SYMBOL	PARAMETER	MIN	MAX	UNIT
tAR	Address Stable Before READ	30		ns
tRA	Address Hold Time for READ	5		ns
tRR	READ Pulse Width	300		ns
tRD	Data Delay From READ (1)		200	ns
tDF	READ to Data Floating	25	100	ns
tRV	Recovery Time Between READ and Any Other Control Signal	1		us

WRITE

SYMBOL	PARAMETER	MIN	MAX	UNIT
tAW	Address Stable Before *WRITE	30		ns
tWA	Address Hold Time for *WRITE	30		ns
tWW	*WRITE Pulse Width	300		ns
tDW	Data Set Up Time for *WRITE	250		ns
tWD	Data Hold Time for *WRITE	30		ns
tRV	Recovery Time Between *WRITE and Any Other Control Signal	1		us

CLOCK AND GATE TIMING

SYMBOL	PARAMETER	MIN	MAX	UNIT
tCLK	Clock Period	380	dc	ns
tPWH	High Pulse Width	230		ns
tPWL	Low Pulse Width	150		ns
tGW	Gate Width High	150		ns
tGL	Gate Width Low	100		ns
tGS	Gate Set Up Time to CLK ↑	100		ns
tGH	Gate Hold Time After CLK ↑	50		ns
tOD	Output Delay from CLK (1)		400	ns
tODG	Output Delay from Gate (1)		300	ns

1. Test Conditions: CL = 150 pF
2. AC Timings measured at VOH 2.2V, VOL 0.8V.

6.5 8255A-5 - PROGRAMMABLE PERIPHERAL INTERFACE

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias .. .. 0 to 70 degC
Storage Temperature .. .. -65 to +150 degC
Voltage On Any Pin WRT Ground .. .. -0.5V to +7V
Power Dissipation .. .. 1 W

D.C. CHARACTERISTICS (TA = 0 to 70 degC, VCC = +5V ±5%, GND = 0V)

SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITIONS
VIL	Input Low Voltage	-0.5	0.8	V	
VIH	Input High Voltage	2.0	VCC	V	
VOL(DB)	Output Low Voltage (Data Bus)		0.45	V	IOL = 2.5 mA
VOL(PER)	Output Low Voltage (Peripheral Port)		0.45	V	IOL = 1.7 mA
VOH(DB)	Output High Voltage (Data Bus)	2.4		V	IOH = -400 uA
VOH(PER)	Output High Voltage (Peripheral Port)	2.4		V	IOH = -200 uA
IDAR (1)	Darlington Drive Current	-1.0	-4.0	mA	REXT=750Ω,VEXT=1.5V
ICC	Power Supply Current		120	mA	
IIL	Input Load Current		±10	uA	VIN = VCC to 0V
IOFL	Output Float Leakage		±10	uA	VOUT = VCC to .45V

1. Available on any 8 pins from Ports B and C

CAPACITANCE (TA = 25 degC, VCC = GND = 0V)

SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITIONS
CIN	Input Capacitance		10	pF	fc = 1 MHz
CI/O	I/O Capacitance		20	pF	unmeasured pins GND

A.C. CHARACTERISTICS (TA = 0 to 70 degC, VCC = +5V ±5%, GND = 0V)

Bus Parameters

READ

SYMBOL	PARAMETER	MIN	MAX	UNIT
tAR	Address Stable Before READ	0		ns
tRA	Address Stable After READ	0		ns
tRR	READ Pulse Width	300		ns
tRD	Data Valid From READ (1)		200	ns
tDF	Data Float After READ	10	100	ns
tRV	Time Between READs and/or WRITEs	850		ns

WRITE

SYMBOL	PARAMETER	MIN	MAX	UNIT
tAW	Address Stable Before WRITE	0		ns
tWA	Address Stable After WRITE	20		ns
tWW	WRITE Pulse Width	300		ns
tDW	Data Valid to WRITE (T.E)	100		ns
tWD	Data Valid After WRITE	30		ns

OTHER TIMINGS

SYMBOL	PARAMETER	MIN	MAX	UNIT
tWB	WR = 1 to Output (1)		350	ns
tIR	Peripheral Data Before RD	0		ns
tHR	Peripheral Data After RD	0		ns
tAK	ACK Pulse Width	300		ns
tST	STB Pulse Width	500		ns
tPS	Peripheral Data Before T.E of STB	0		ns
tPH	Peripheral Data After T.E of STB	180		ns
tAD	ACK = 0 to Output (1)		300	ns
tKD	ACK = 1 to Output Float	20	250	ns
tWOB	WR = 1 to OBF = 0 (1)		650	ns
tAOB	ACK = 0 to OBF = 1 (1)		350	ns
tSIB	STB = 0 to IBF = 1 (1)		300	ns
tRIB	RD = 1 to IBF = 0 (1)		300	ns
tRIT	RD = 0 to INTR = 0 (1)		400	ns
tSIT	STB = 1 to INTR = 1 (1)		300	ns
tAIT	ACK = 1 to INTR = 1 (1)		350	ns
tWIT	WR = 0 to INTR = 0 (1,3)		450	ns

1. Test Conditions: CL = 150 pF
2. Period of Reset pulse must be at least 50 us during or after power on. Subsequent Reset pulse can be 500 ns min.
3. INTR may occur as early as *WR.

6.6 8259A - PROGRAMMABLE INTERRUPT CONTROLLER

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias .. .. 0 to 70 degC
Storage Temperature .. .. -65 to +150 degC
Voltage On Any Pin WRT Ground .. .. -0.5V to +7V
Power Dissipation .. .. 1 W

D.C. CHARACTERISTICS (TA = 0 to 70 degC, VCC = +5V ±10%)

SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITIONS
VIL	Input Low Voltage	-0.5	0.8	V	
VIH	Input High Voltage	2.0	VCC+.5V	V	
VOL	Output Low Voltage		0.45	V	IOL = 2.2 mA
VOH	Output High Voltage	2.4		V	IOH = -400 uA
VOH(INT)	Output High Voltage (Interrupt)	3.5 2.4		V V	IOH = -100 uA IOH = -400 uA
ILI	Input Load Current	-10	+10	uA	0V < VIN < VCC
ILOL	Output Leakage Current	-10	+10	uA	.45V < VOUT < VCC
ICC	VCC Supply Current		85	mA	
ILIR	IR Input Load Current		-300 10	uA uA	VIN = 0 VIN = VCC

CAPACITANCE (TA = 25 degC, VCC = GND = 0V)

SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITIONS
CIN	Input Capacitance		10	pF	fc = 1 MHz
CI/O	I/O Capacitance		20	pF	unmeasured pins GND

A.C. CHARACTERISTICS (TA = 0 to 70 degC, VCC = +5V ±10%)

TIMING REQUIREMENTS

SYMBOL	PARAMETER	MIN	MAX	UNIT
TAHRL	AO/*CS Set Up to *RD/*INTA ↓	0		ns
TRHAX	AO/*CS Hold After *RD/*INTA ↑	0		ns
TRLRH	*RD Pulse Width	235		ns
TAHWL	AO/*CS Set Up to *WR ↓	0		ns
TWHAX	AO/*CS Hold After *WR ↑	0		ns
TWLWH	*WR Pulse Width	290		ns
TDVWH	Data Set Up to *WR ↑	240		ns
TWHDX	Data Hold After *WR ↑	0		ns
TJLJH	Interrupt Request Width (Low) (1)	100		ns
TCVIAL	Cascade Set Up to Second or Third *INTA Slave only	55		ns
TRHRL	End of *RD to Next *RD End of *INTA to Next *INTA within an *INTA sequence only	160		ns
TWHWL	End of *WR to Next *WR	190		ns
TCHCL	End of Command to Next Command (Not same command type) End of *INTA to next *INTA Sequence	500		ns

1. This is the low time required to clear the input latch in the edge triggered mode
2. Worst case timing for TCHCL in actual uP system is typically much greater than 500 ns

TIMING RESPONSES

SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITIONS
TRLDV	Data Valid from *RD/*INTA ↓		200	ns	C of Data Bus = 100 pF
TRHDZ	Data Float After *RD/*INTA ↑		100	ns	
TJHIH	Interrupt Output Delay		350	ns	C of Data Bus Max test C = 100 pF Min test C = 15 pF
TIALCV	Cascade Valid from First *INTA ↓ (Master Only)		565	ns	CINT = 100 pF
TRLEL	Enable Active from *RD or *INTA ↓		125	ns	Ccascade = 100 pF
TRHEH	Enable Inactive from *RD or *INTA ↑		150	ns	
TAHDV	Data Vaid from Stable Address		200	ns	
TCVDV	Cascade Valid to Valid Data		300	ns	

6.7 FD1797 - FLOPPY DISK FORMATTER/CONTROLLER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature .. .. 0 to 70 degC
Storage Temperature .. .. -55 to +125 degC
Supply Voltage VDD WRT VSS .. .. -0.3V to +15V
Voltage on any Input WRT VSS .. .. -0.3V to +15V

D.C. CHARACTERISTICS (TA = 0 to 70 degC, VDD = +12V ±.6V, VSS = 0V VCC = +5V ±.25V)

SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITIONS
IIL	Input Leakage		10	uA	VIN = VDD
IOL	Output Leakage		10	uA	VOUT = VDD
VIH	Input High Voltage	2.6		V	
VIL	Input Low Voltage		0.8	V	
VOH	Output High Voltage	2.8		V	IO = -100 uA
VOL	Output Low Voltage		0.45	V	IO = 1.6 mA
PD	Power Dissipation		500	mW	

TIMING CHARACTERISTICS (TA = 0 to 70 degC, VDD = +12V ±.6V, VSS = 0V VCC = +5V ±.25V)

READ ENABLE TIMING

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
TSET	Set Up ADDR and CS to *RE	50			ns	
THLD	Hold ADDR and CS from *RE	10			ns	
TRE	*RE Pulse Width	400			ns	CL = 50 pF
TDRR	DRQ Reset from *RE		400	500	ns	
TIRR	INTRQ Reset from *RE		500	3000	ns	Note 5
TDACC	Data Access from *RE			350	ns	CL = 50 pF
TDOH	Data Hold from *RE	50		150	ns	CL = 50 pF

WRITE ENABLE TIMING

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
TSET	Set Up ADDR and CS to *WE	50			ns	
THLD	Hold ADDR and CS from *WE	10			ns	
TWE	*WE Pulse Width	350			ns	
TDRR	DRQ Reset from *WE		400	500	ns	
TIRR	INTRQ Reset from *WE		500	3000	ns	Note 5
TDS	Data Set Up to *WE	250			ns	
TDH	Data Hold from *WE	70			ns	

INPUT DATA TIMING

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
Tpw	*Raw Read Pulse Width	100	200		ns	Note 1
tbc	*Raw Read Cycle Time		1500		ns	1800 ns at 70 degC
Tc	RCLK Cycle Time		1500		ns	
Tx1	RCLK Hold to *Raw Read	40			ns	Note 1
Tx2	*Raw Read Hold to RCLK	40			ns	

WRITE DATA TIMING (All Double When CLK = 1 MHz)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
Twp	Write Data Pulse Width	450 150	500 200	550 250	ns ns	FM MFM
Twg	Write Gate to Write Data		2 1		us us	FM MFM
Tbc	Write Data Cycle Time		2,3,4		us	±CLK Error
Ts	Early(Late) to Write Data	125			ns	MFM
Th	Early(Late) from Write Data	125			ns	MFM
Twf	Write Gate Off from WD		2 1		us us	FM MFM
Twd1	WD Valid to CLK	100 50			ns ns	CLK = 1 MHz CLK = 2 MHz
Twd2	WD Valid After CLK	100 30			ns ns	CLK = 1 MHz CLK = 2 MHz

MISCELLANEOUS TIMING

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
TCD1	Clock Duty Low	230	250	20000	ns	
TCD2	Clock Duty High	200	250	20000	ns	
TSTP	Step Pulse Output	2 or 4			us	Note 5
TDIR	Dir Set Up to Step		12		us	±CLK Error
TMR	Master Reset Pulse Width	50			us	Note 5
TIP	Index Pulse Width	10			us	Note 5
TWF	Write Fault Pulse Width	10			us	

1. Pulse Width on Raw Read pin is normally 100-300 ns. However pulse may be any width if pulse is entirely within window. If pulse occurs in both windows, then pulse width must be less than 300 ns for MFM at CLK = 2 MHz and 600 ns for FM at 2 MHz. Times double for 1 MHz.
2. A PPL Data Separator is recommended for 8in MFM.
3. tbc should be 2 us nominal in MFM and 4 us nominal in FM. Times double when CLK = 1 MHz.
4. RCLK may be high or low during RAW READ.
5. Times double when clock = 1 MHz.

6.8 WD1691 - FLOPPY SUPPORT LOGIC

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias .. .. -25 to +70 degC
Storage Temperature (Ceramic) .. .. -65 to +150 degC
Storage Temperature (Plastic) .. .. -55 to +125 degC
Voltage On Any Pin WRT VSS .. .. -0.2V to +7V
Power Dissipation .. .. 1 W

D.C. CHARACTERISTICS (TA = 0 to 70 degC, VCC = +5V ±10%, VSS = 0V)

SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITIONS
VIL	Input Low Voltage	-0.2	0.8	V	
VIH	Input High Voltage	2.0		V	
VOL	Output Low Voltage		0.45	V	IOL = 3.2 mA
VOH	Output High Voltage	2.4		V	IOH = -200 uA
VCC	Supply Voltage	4.5	5.5	V	
ICC	Supply Current		100	mA	All Outputs Open

A.C. CHARACTERISTICS (TA = 0 to 70 degC, VCC = +5V ±10%, VSS = 0V)

SYMBOL	PARAMETER	MIN	MAX	UNIT
FIN	VCO Input Frequency (*DDEN = 0 or 1)	0.5	6	MHz
Rpw	*RDD Pulse Width	100		ns
Wel	EARLT (LATE) to WDIN	100		ns
Pon	PUMP UP/DN Time	0	250	ns
Wpi	WDIN to WDOUT (*DDEN = 1)		80	ns
INR	Internal Pull-up Resistor	4.0	10	KΩ

6.9 MC6845 - CRT CONTROLLER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature .. .. 0 to 70 degC
Storage Temperature .. .. -55 to +150 degC
Supply Voltage WRT VSS .. .. -0.3V to +7V
Input Voltage WRT VSS .. .. -0.3V to +7V

CHARACTERISTICS (TA = 0 to 70 degC, VCC = +5V ±5%, VSS = 0V)

D.C.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
VIL	Input Low Voltage	-0.3		0.8	V
VIH	Input High Voltage	2.0		VCC	V
Iin	Input Leakage Current		1.0	2.5	uA
ITSI	Three-state (VCC=5.25V) (Vin = 0.4 to 2.4V)	-10	2.0	10	uA
VOH	Output High Voltage (Iload = -205 uA) D0-D7 (Iload = -100 uA) Other Outputs	 2.4 2.4			 V V
VOL	Output Low Voltage (Iload = 1.6 mA)			0.4	V
PD	Power Dissipation		600		mW

CAPACITANCE

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
Cin	Input Capacitance	D0-D7			12.5	pF
		All Others			10	pF
Cout	Output Capacitance				10	pF

A.C.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
PWCL	Minimum Clock Pulse Width Low	160			ns
PWCH	Minimum Clock Pulse Width High	200			ns
fc	Clock Frequency			2.5	MHz
tcr,tcf	Rise and Fall Time for Clock Input			20	ns
tMAD	Memory Address Delay Time			160	ns
tRAD	Raster Address Delay Time			160	ns
tDTD	Display Timing Delay Time			300	ns
tHSD	Horizontal Sync Delay Time			300	ns
tVSD	Vertical Sync Delay Time			300	ns
tCDD	Cursor Display Timing Delay Time			300	ns
PWLPD	Light Pen Strobe Minimum Pulse Width	100			ns
tLPD1	Light Pen Strobe Disable Time			120	ns
tLPD2				0	ns

1. The light pen strobe must fall to low level before VSYNC pulse rises.

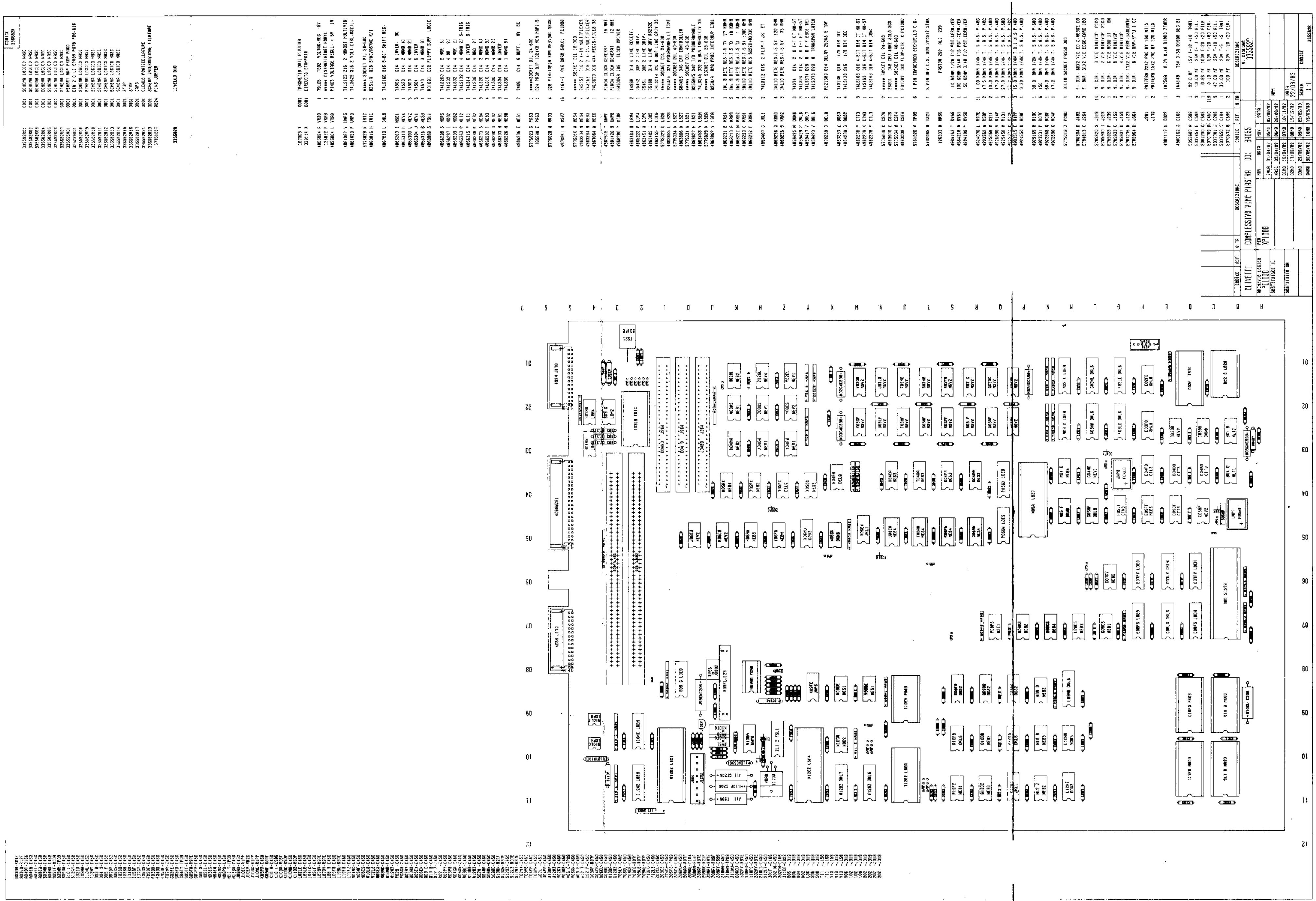
Bus Timing Characteristics

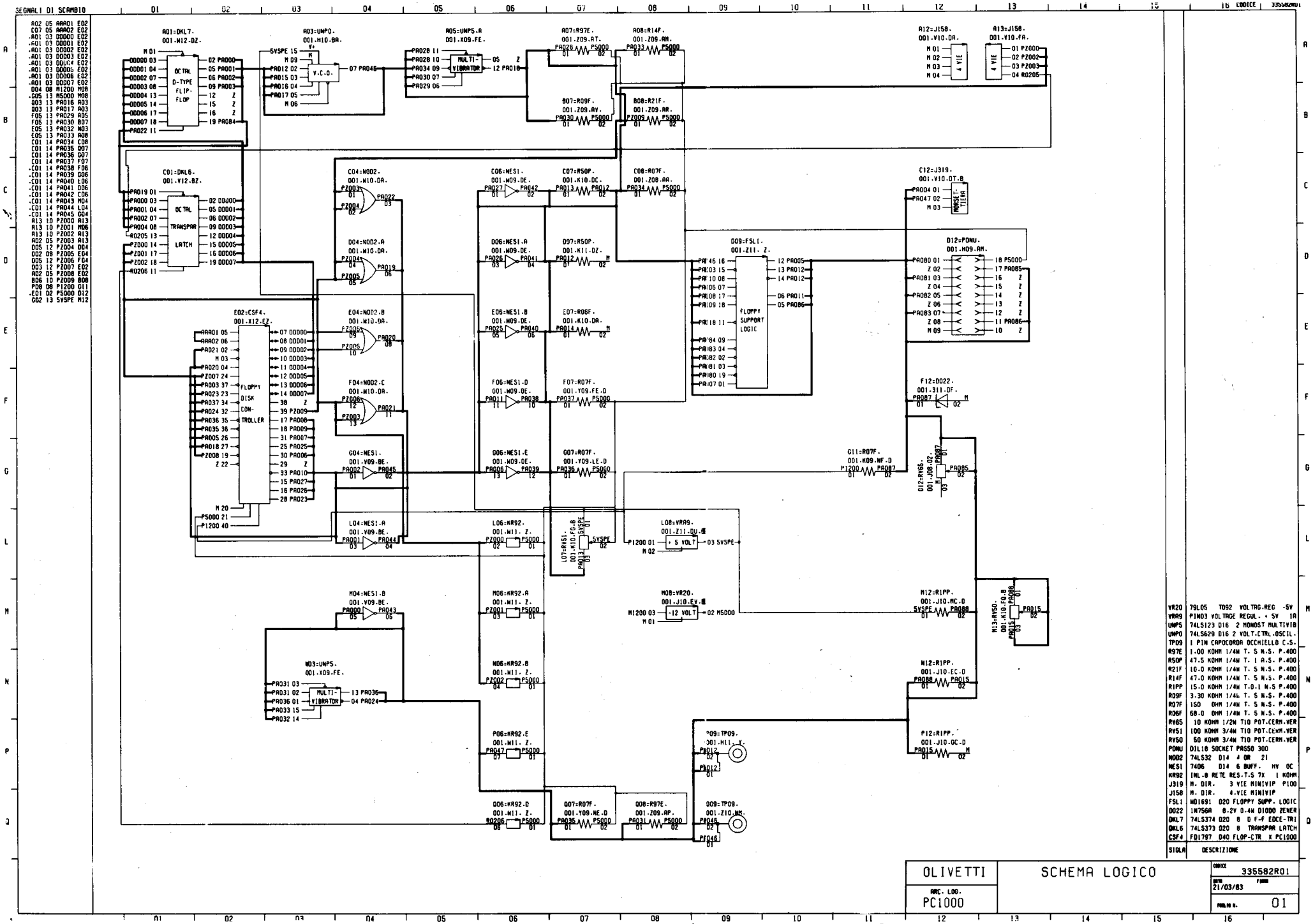
READ/WRITE

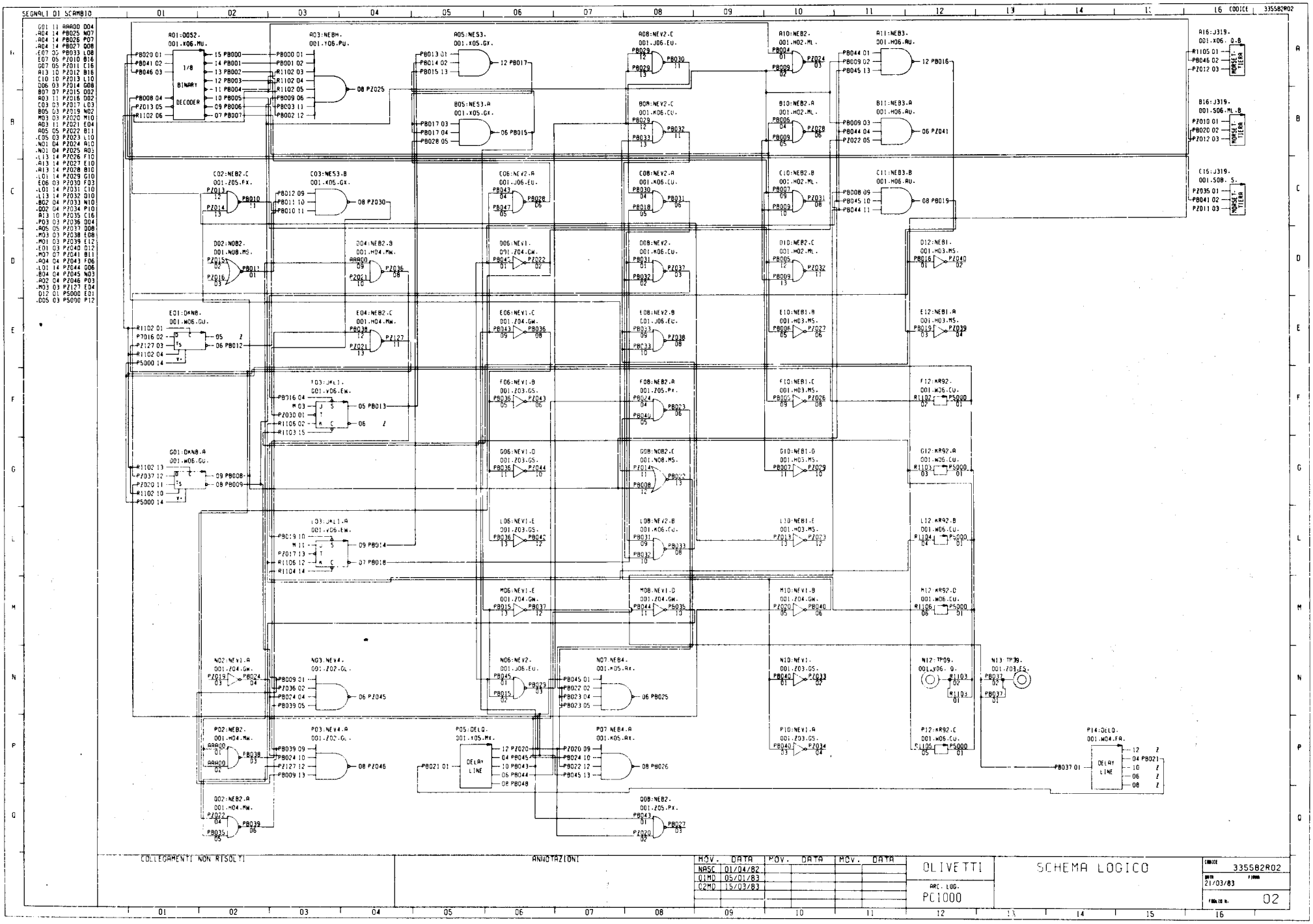
SYMBOL	PARAMETER		MIN	MAX	UNIT
tcycE	Enable Cycle Time		1.0		us
PWEH	Enable Pulse Width High		0.45	25	us
PWEL	Enable Pulse Width Low		0.43		us
tAS	Set Up Time *CS and RS Valid to Enable Positive Transition		160		ns
tDDR	Data Delay Time			320	ns
tH	Data Hold Time	Read	10		ns
		Write	10		ns
tAH	Address Hold Time		10		ns
tEr,tEf	Rise and Fall Time for Enable Input			25	ns
tDSW	Data Set Up Time		195		ns
tACC	Data Access Time			480	ns

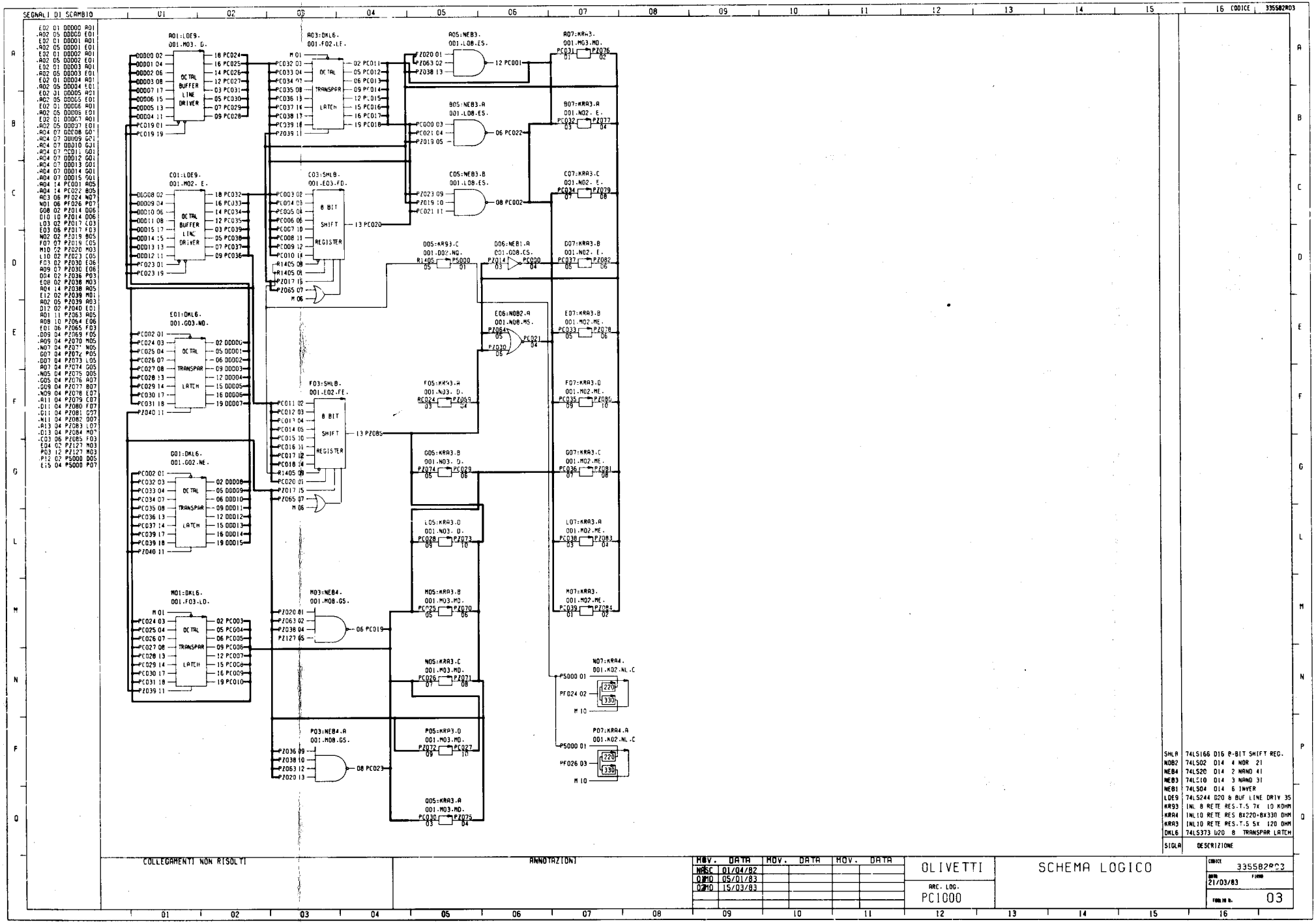
7. LOGIC DIAGRAMS

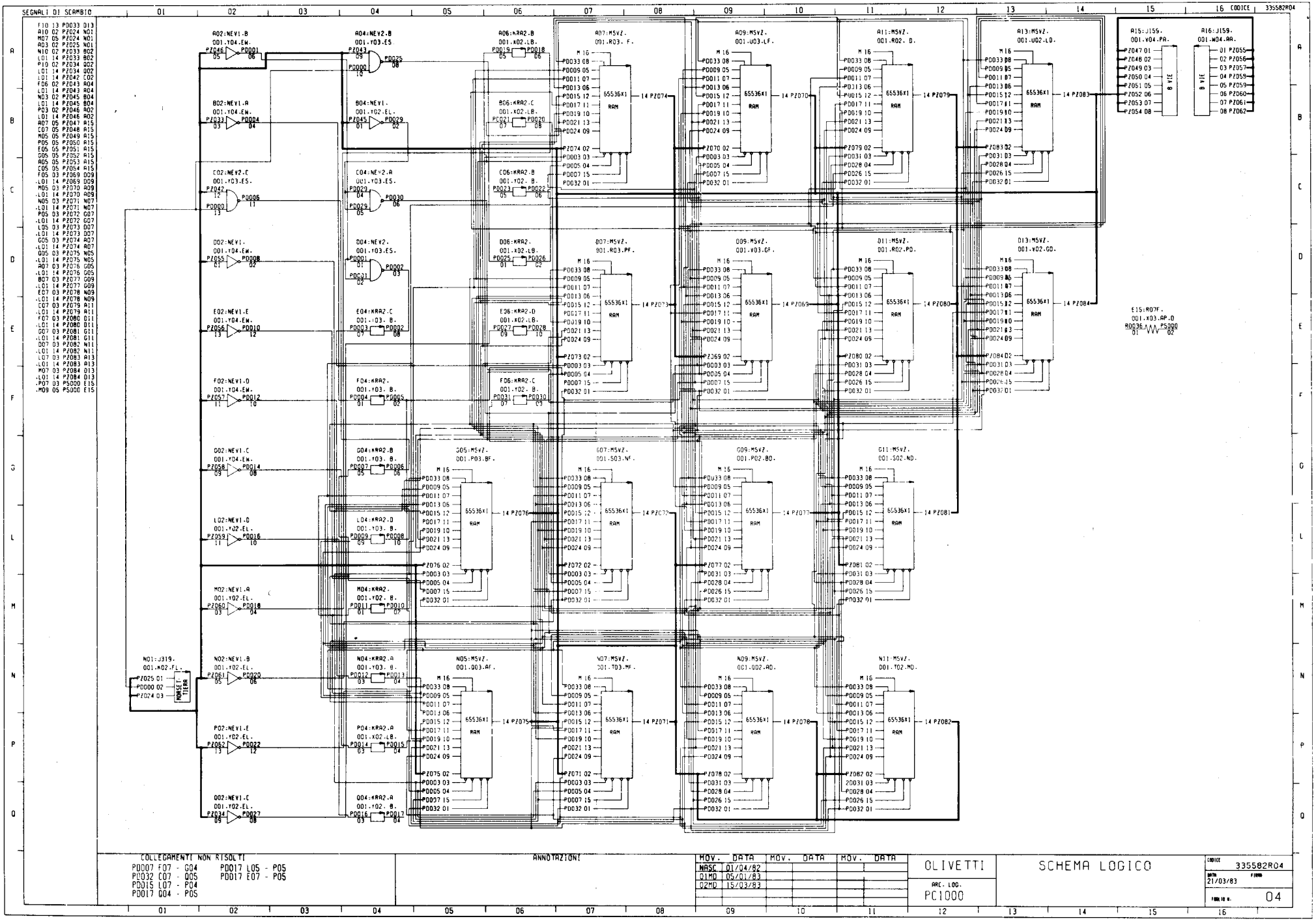
CONTENTS

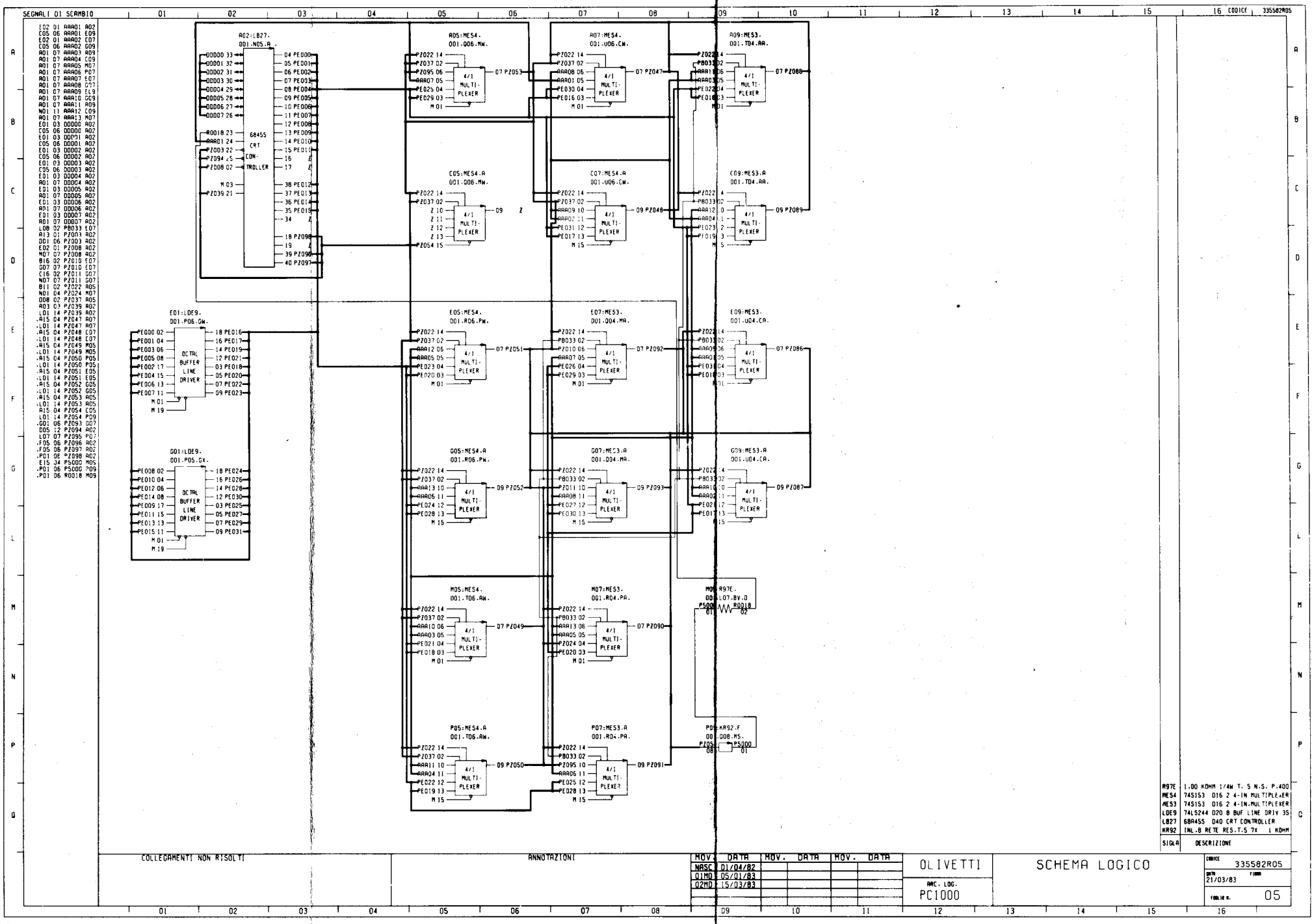


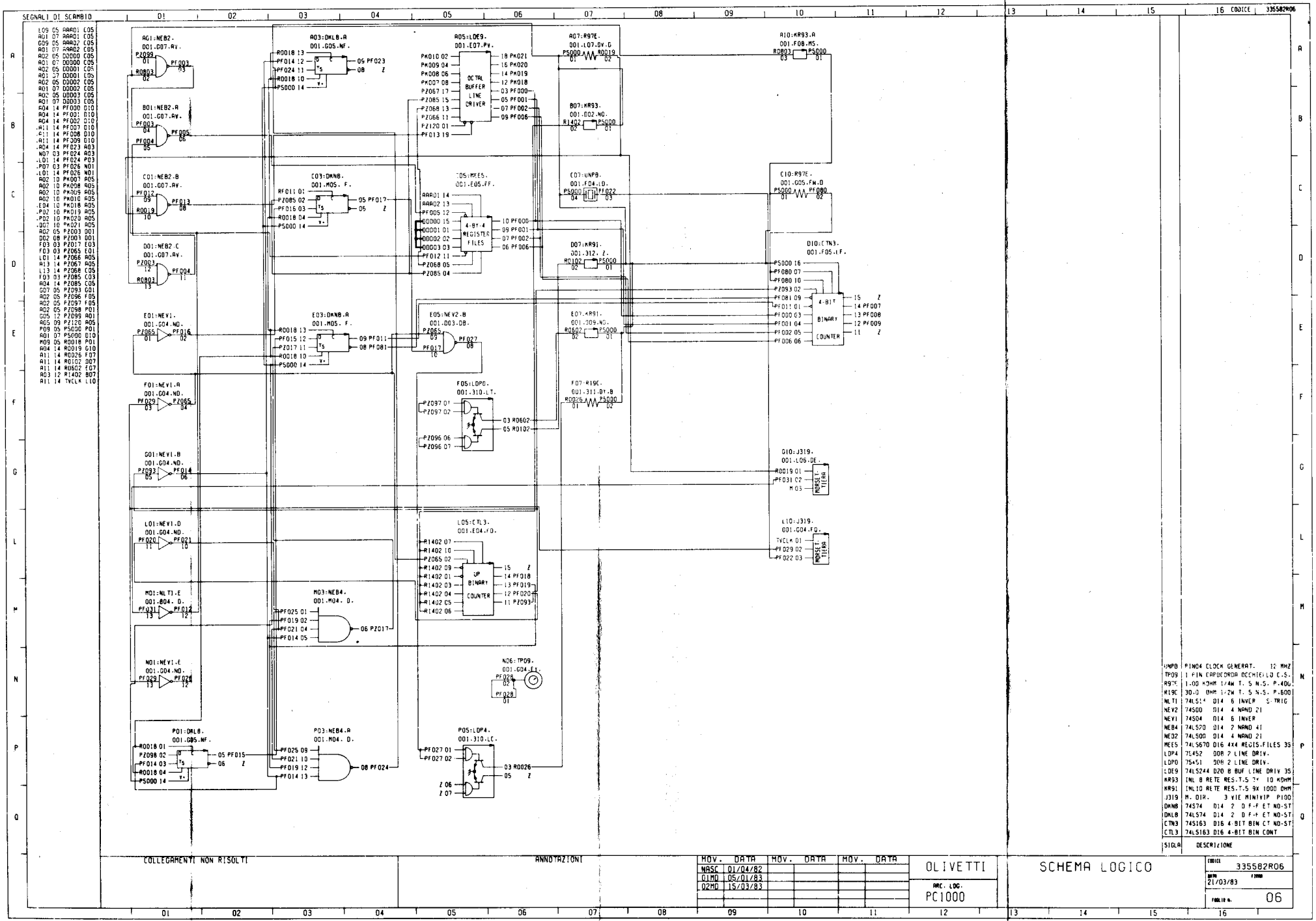






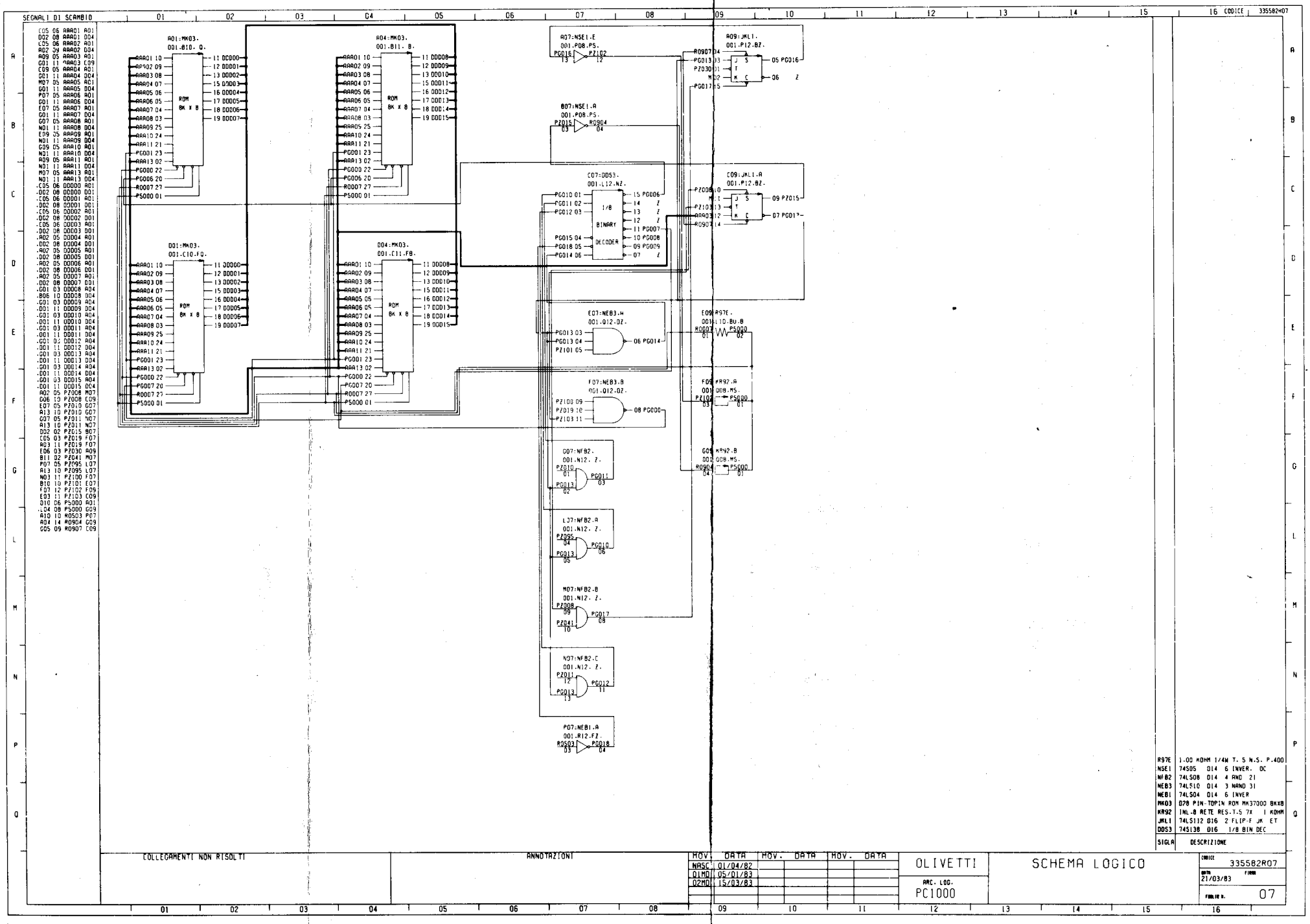


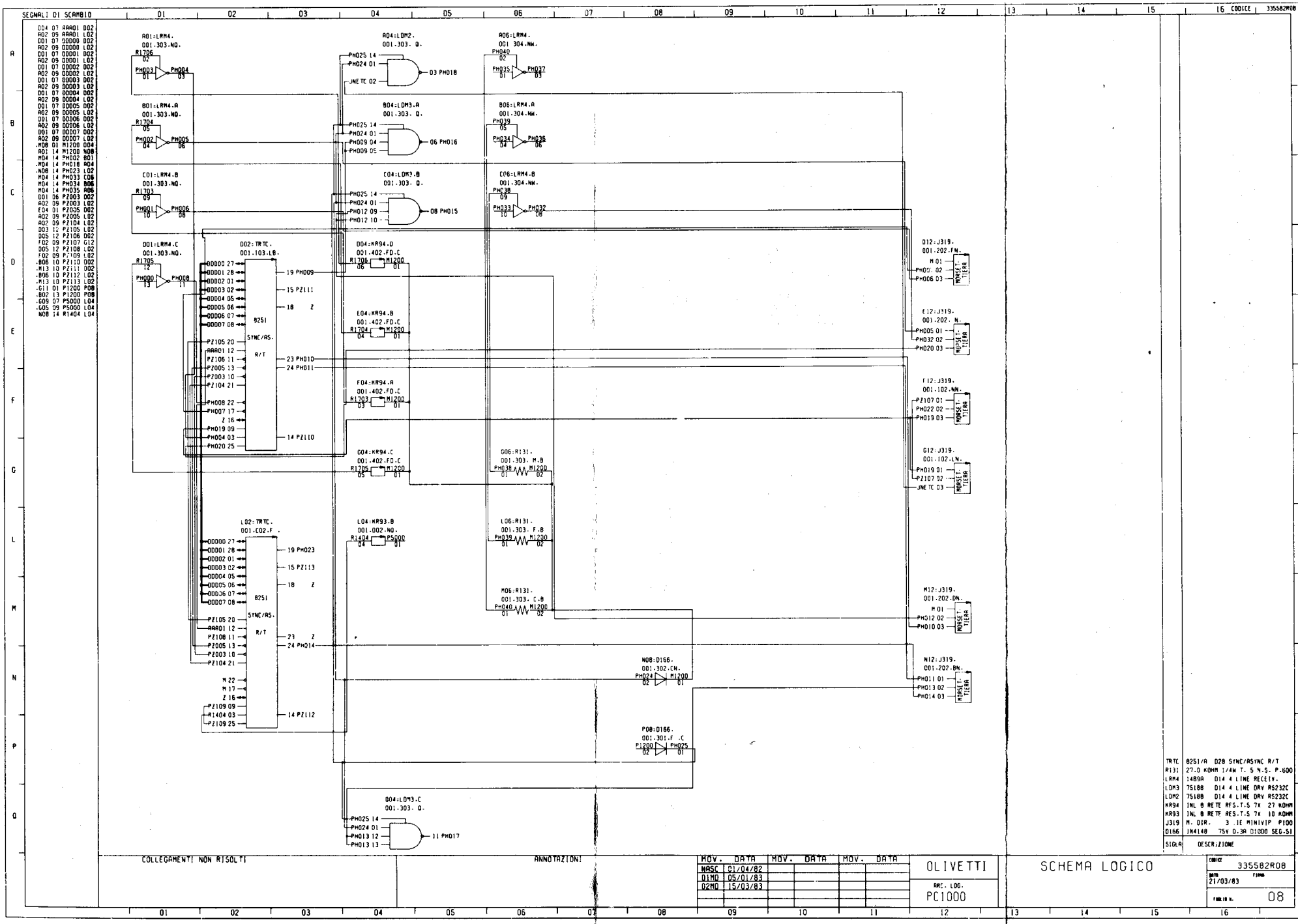


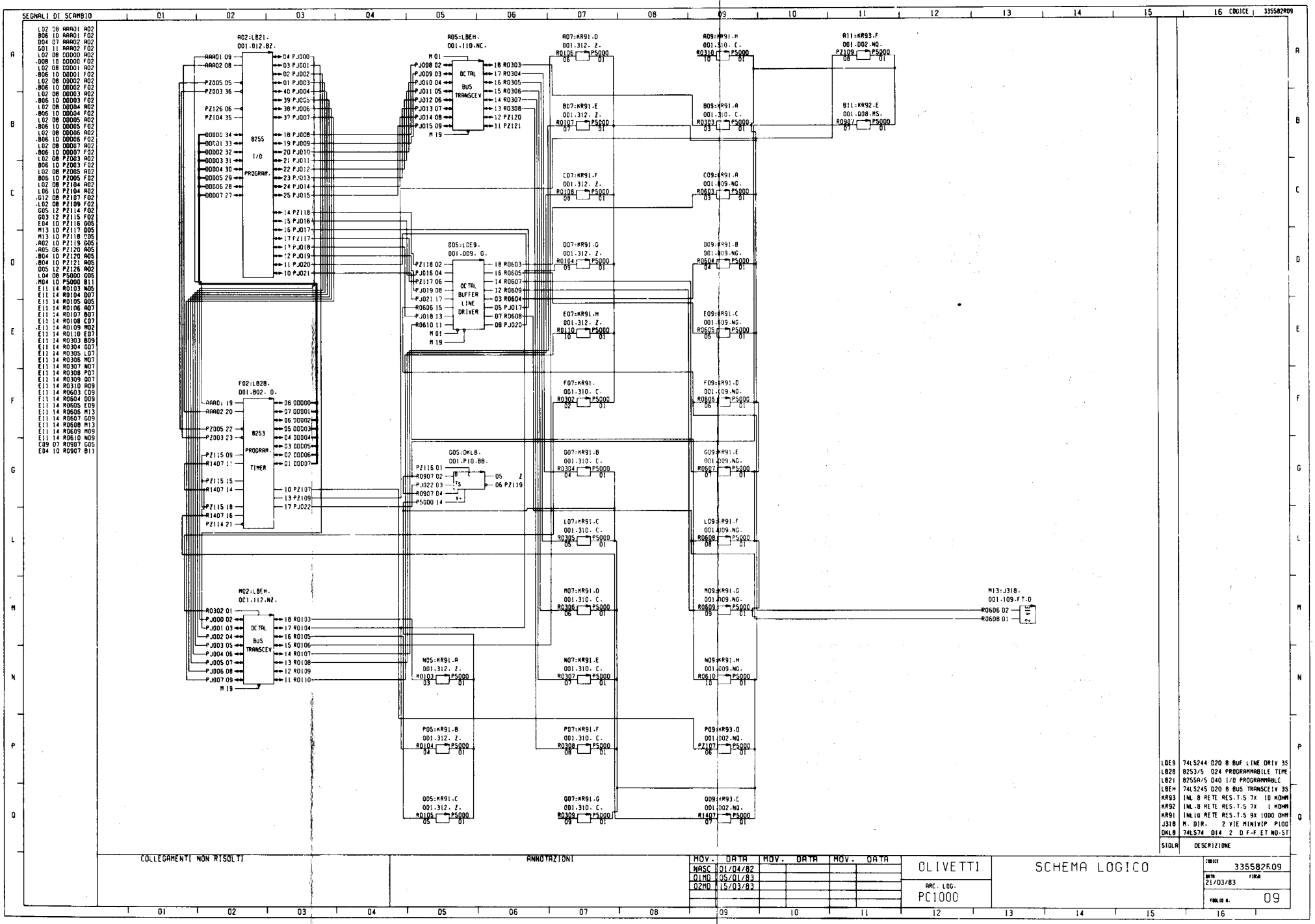


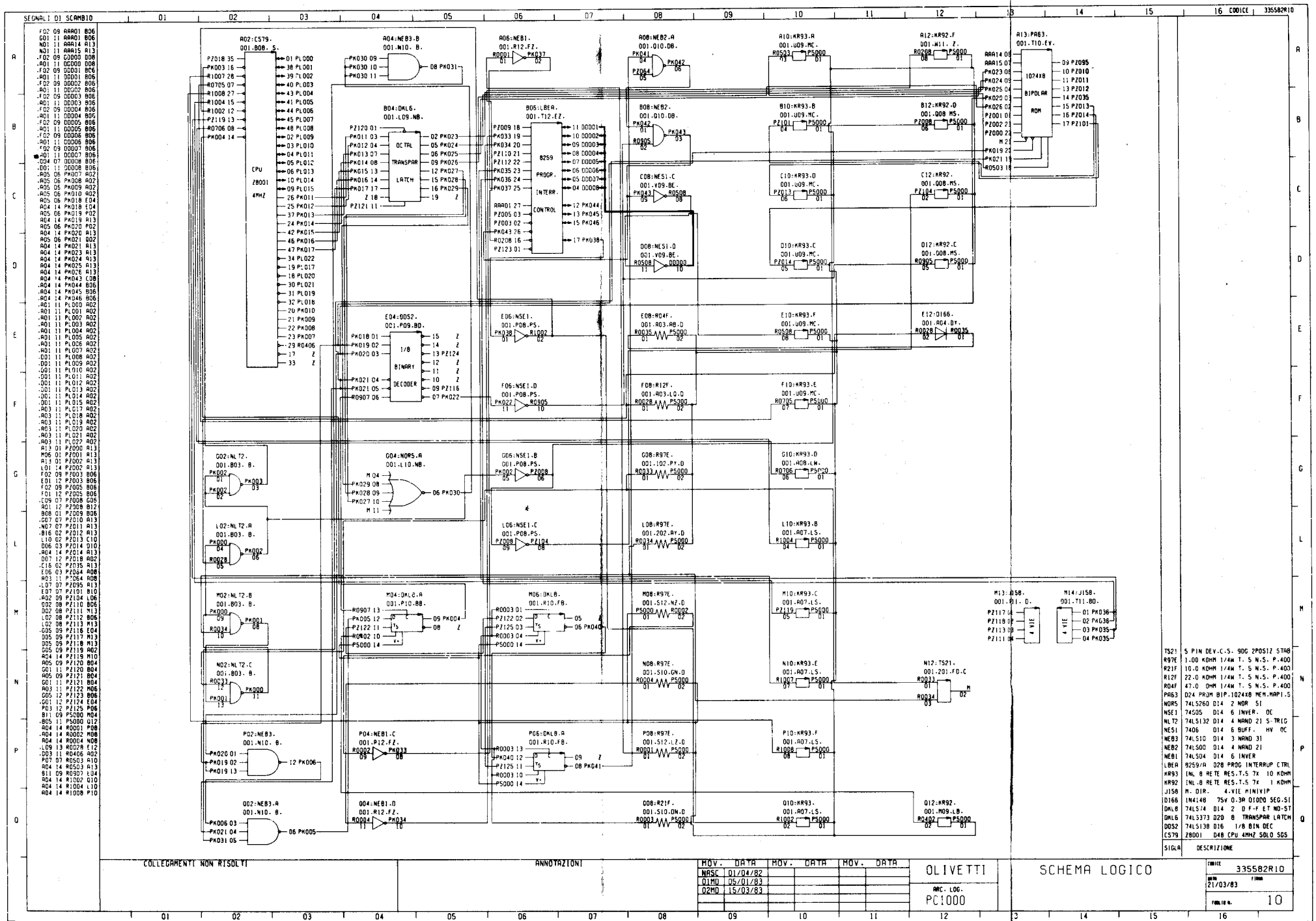
SIGLA	DESCRIZIONE
UNP8	PIN04 CLOCK GENERAT. 12 MHZ
TP09	1 PIN CARDCORDA OCCHIELLO C.S.
R97E	1.00 KOHM 1/4W T. 5 N.S. P.400
R19C	30.0 OHM 1/2W T. 5 N.S. P.600
NLT1	74LS14 D14 6 INVER S-TRIG
NEV2	74S00 D14 4 NAND 2I
NEV1	74S04 D14 6 INVER
NEB4	74LS20 D14 2 NAND 4I
NEB2	74LS00 D14 4 NAND 2I
MEE5	74LS670 D16 4X4 REGIS.FILES 3S
LDP4	75452 DO8 2 LINE DRIV.
LDP0	75451 DO8 2 LINE DRIV.
LDE9	74LS244 D20 8 BUF LINE DRIV 3S
KR93	INL 8 RETE RES.T.5 9X 10 KOHM
KR91	INL10 RETE RES.T.5 9X 1000 OHM
J319	M. DIR. 3 VIE MINIVIP P100
DNB	74S74 D14 2 D F-F ET NO-ST
DRL8	74LS74 D14 2 D F-F ET NO-ST
CTN3	74S163 D16 4-BIT BIN CT NO-ST
CTL3	74LS163 D16 4-BIT BIN CONT

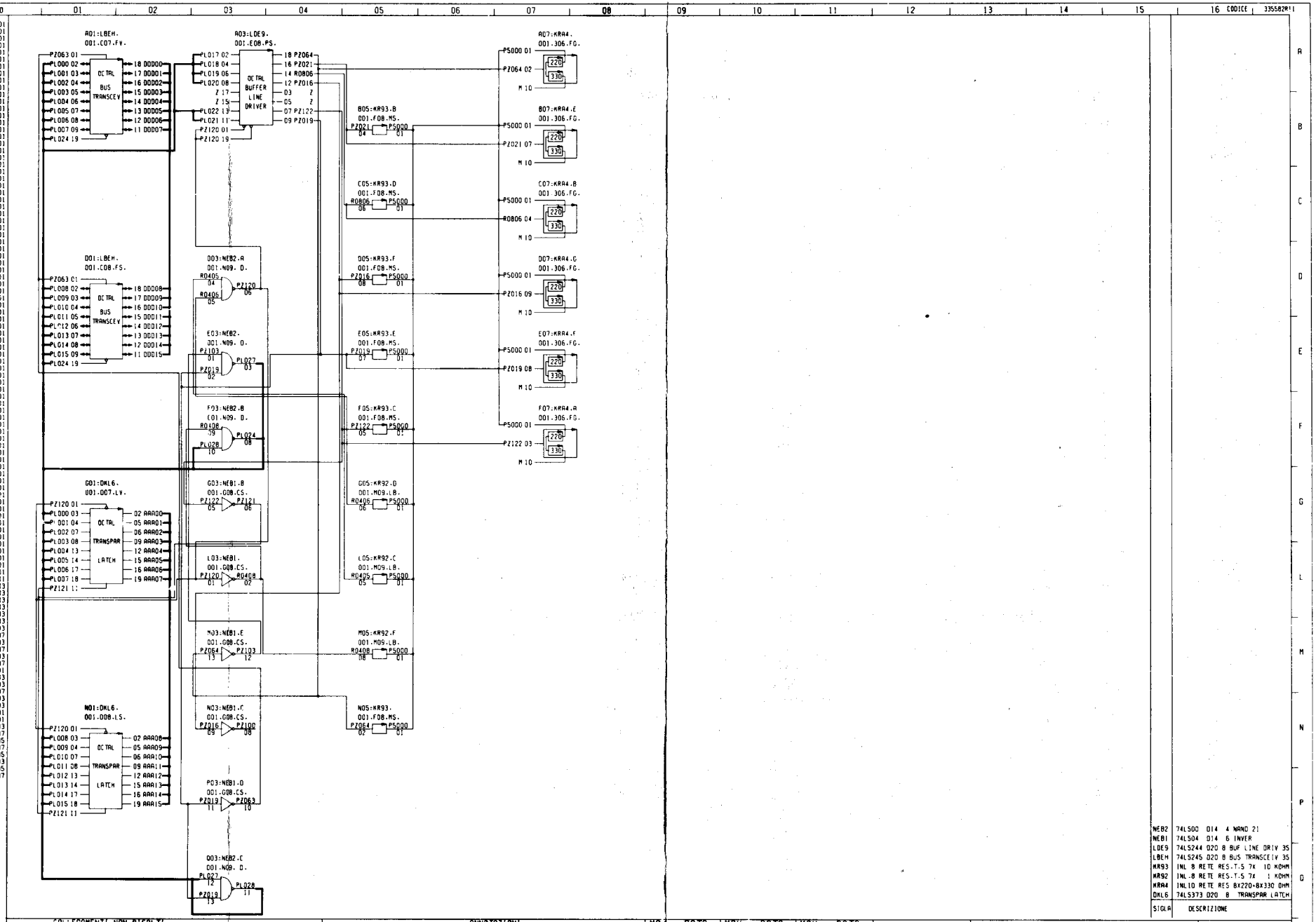
MOV.	DATA
NASC	01/04/82
01MD	05/01/83
02MD	15/03/83

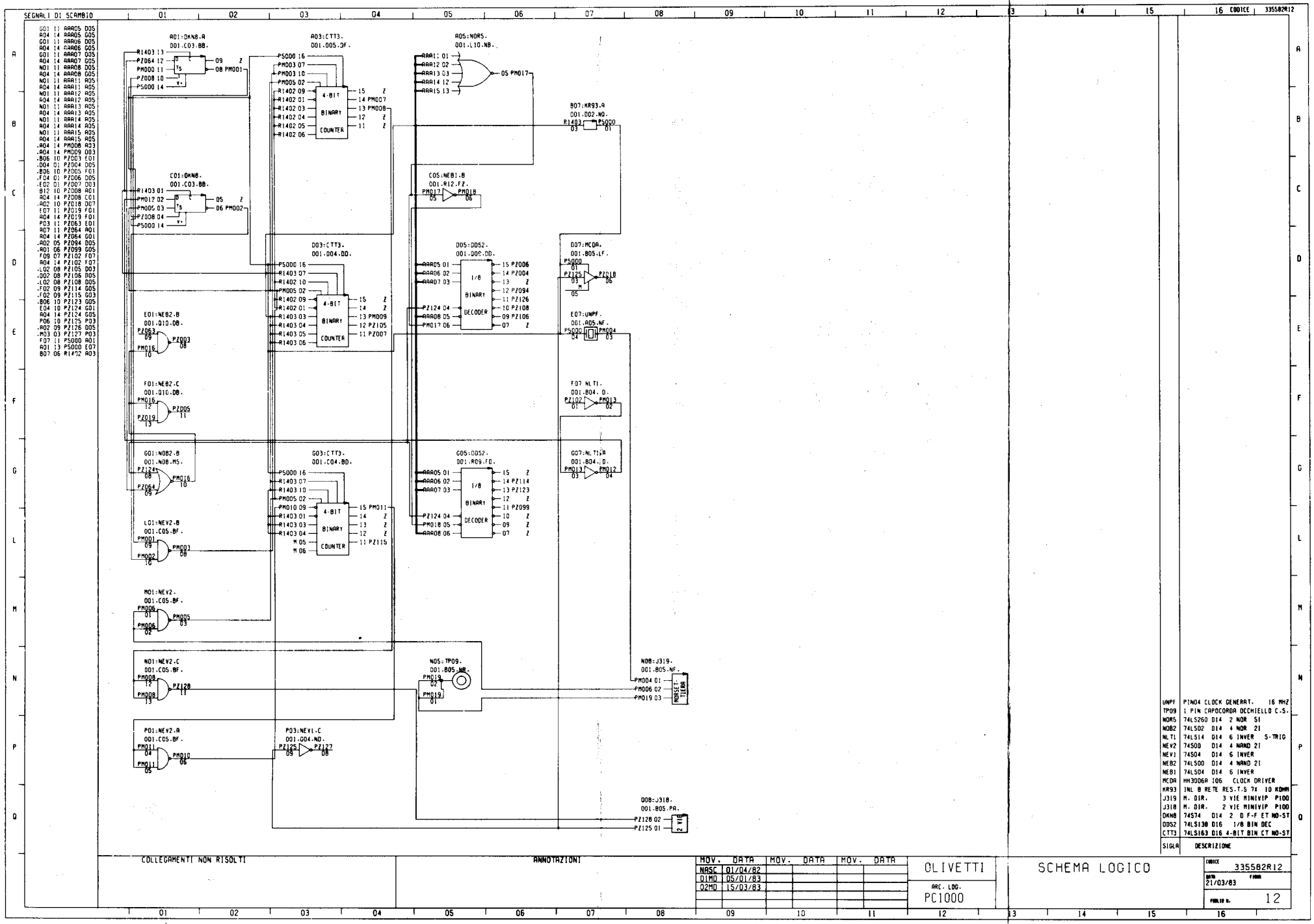


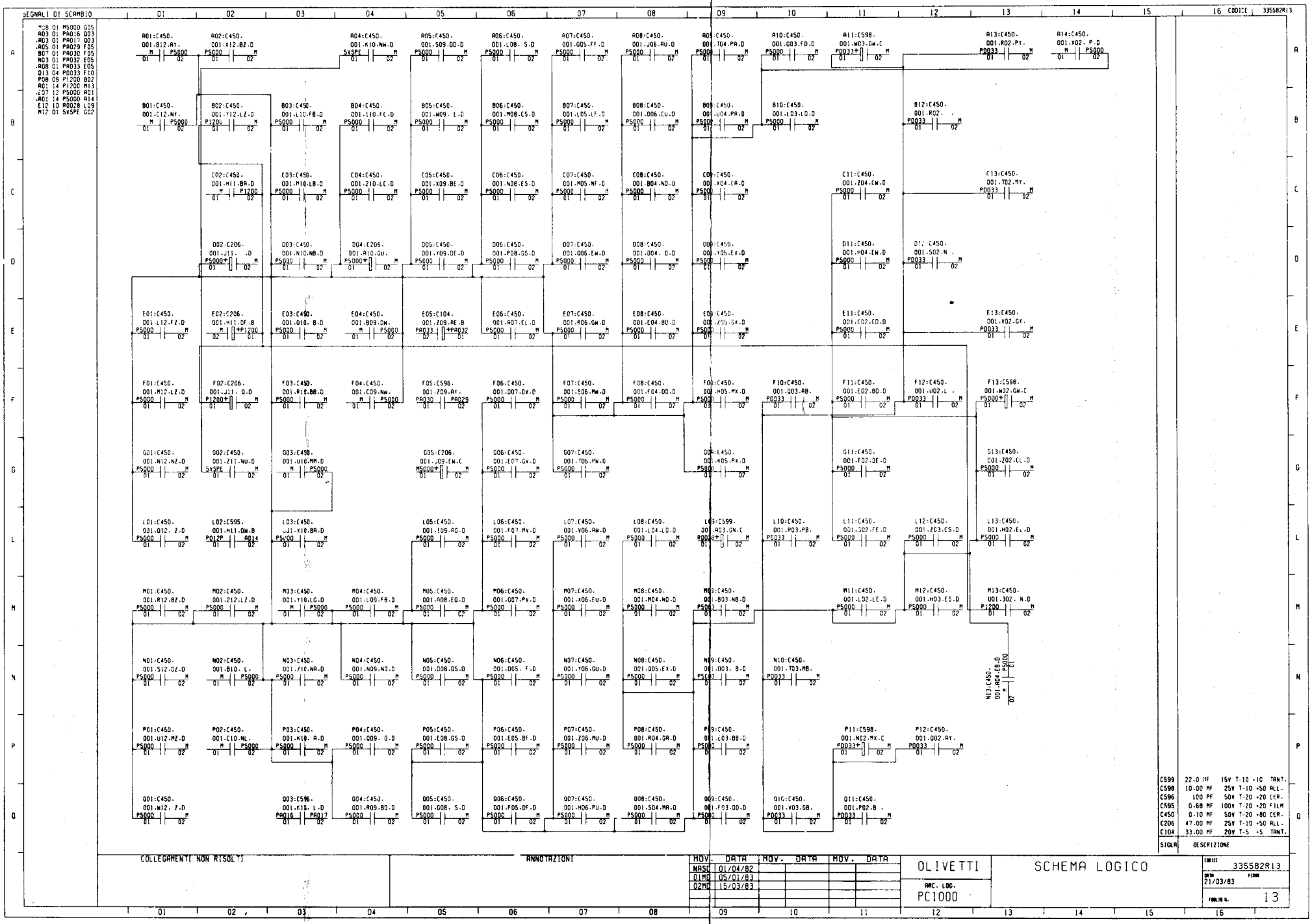


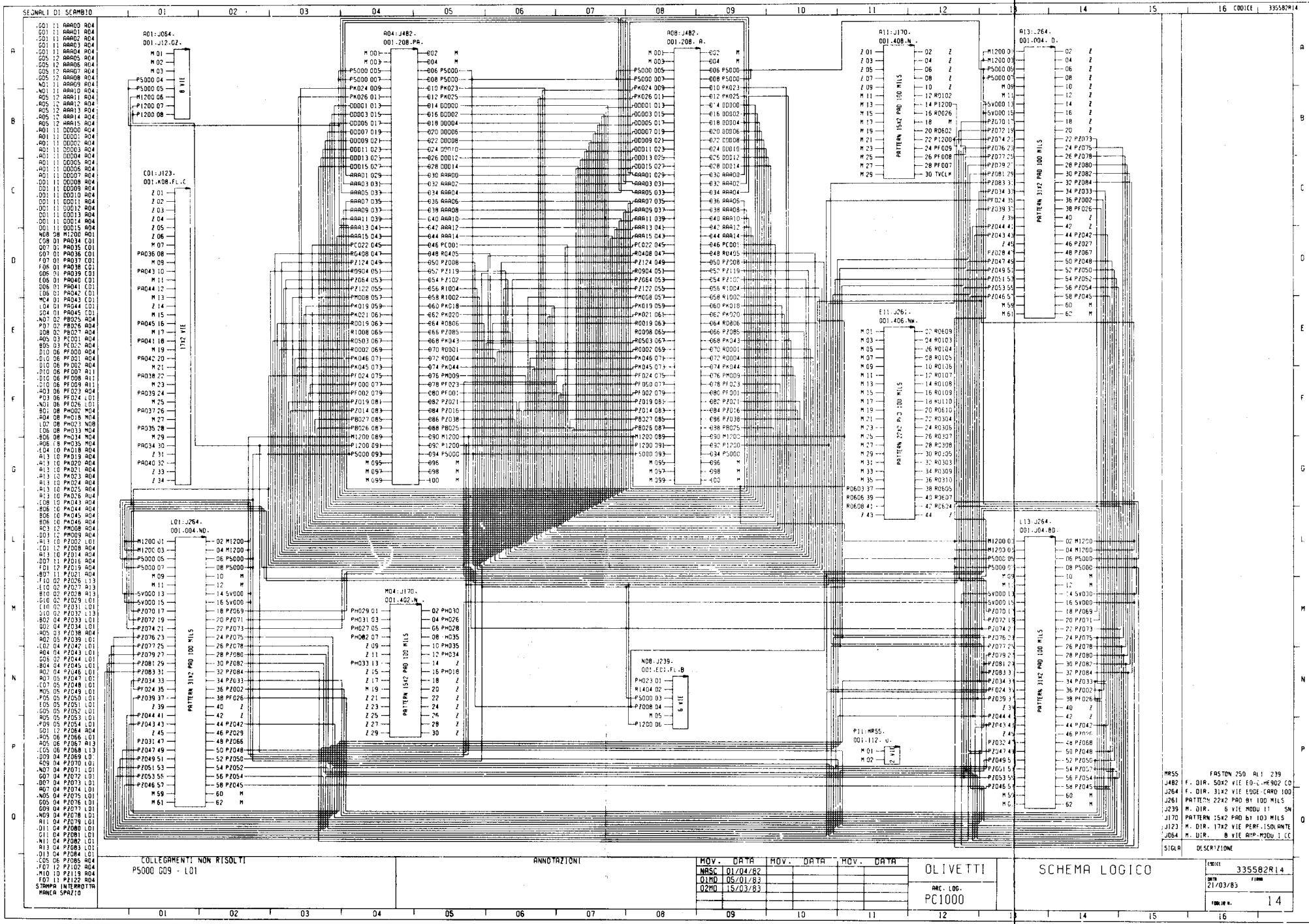








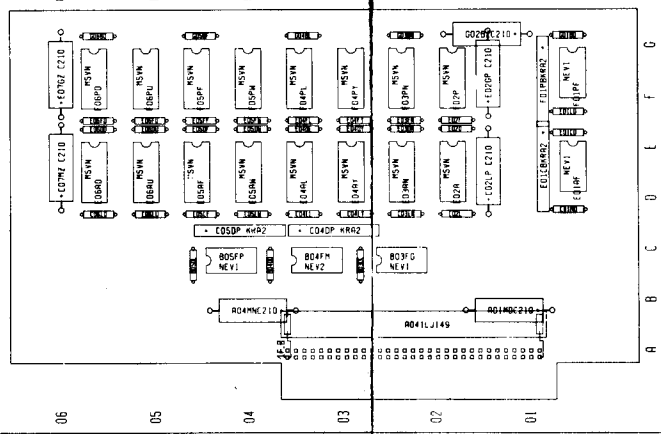




B03DC-C450
B04DD-C450
B05DL-C450
C01MD-C450
C02L -C450
C03LN-C450
C04LL-C450
C04LY-C450
C05LF-C450
C05LW-C450
C06LD-C450
C06LU-C450
E01CD-C450
E01LD-C450
E02D -C450
E02F -C450
E03DN-C450
E03FN-C450
E04DL-C450
E04DT-C450
E04FL-C450
E04FY-C450
E05DF-C450
E05DH-C450
E05FF-C450
E05FN-C450
E06DD-C450
E06DU-C450
E06FD-C450
E06FU-C450
G01BD-C450
G03BN-C450
G04BL-C450
G05BF-C450
G06BD-C450

CODICE 335593L

335593L01 0001 SCHEMA LOGICO
335593L02 0001 SCHEMA LOGICO
335593L03 0001 STIP
335593L04 0001 STRR
335593L05 0001 CAPO

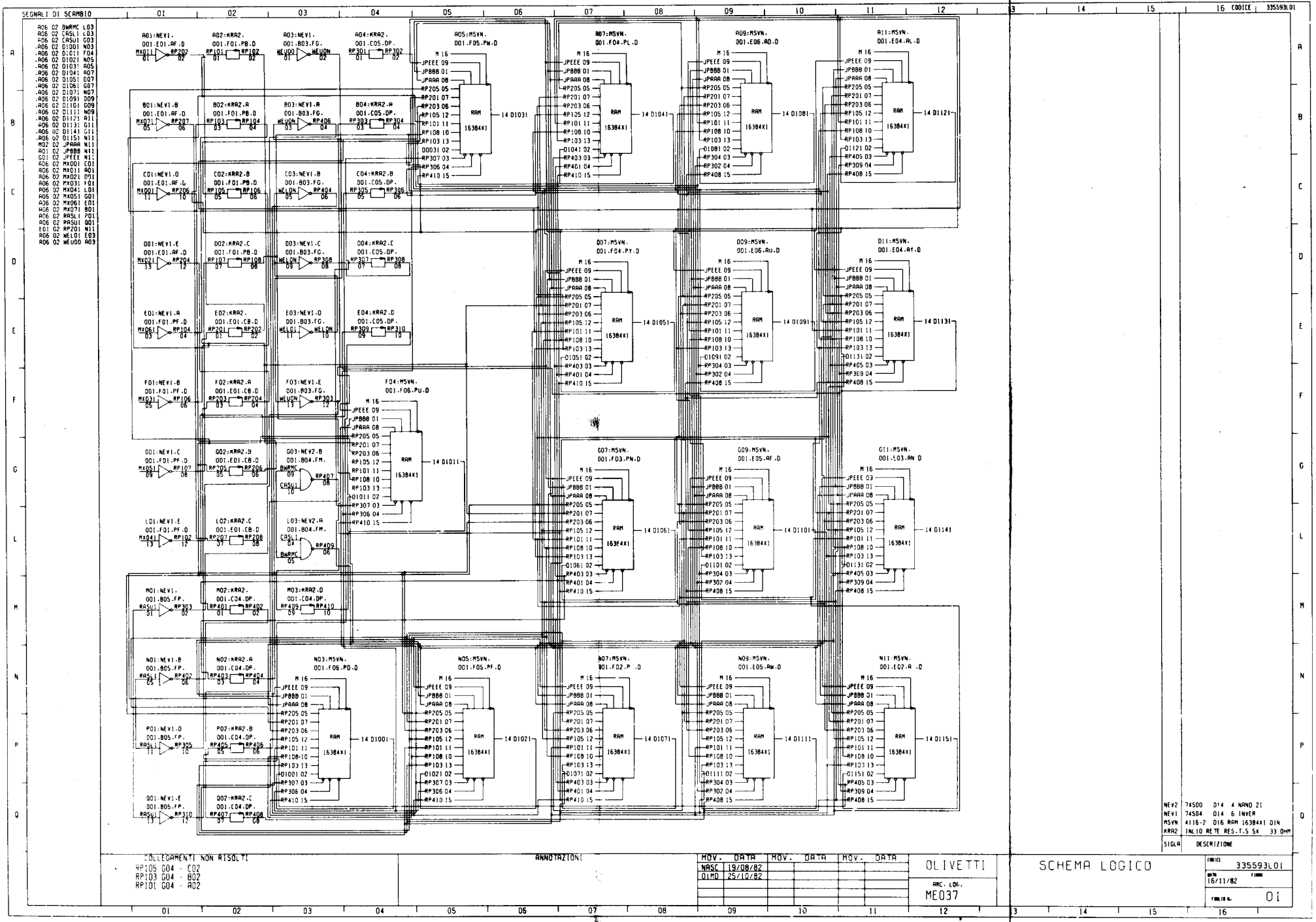


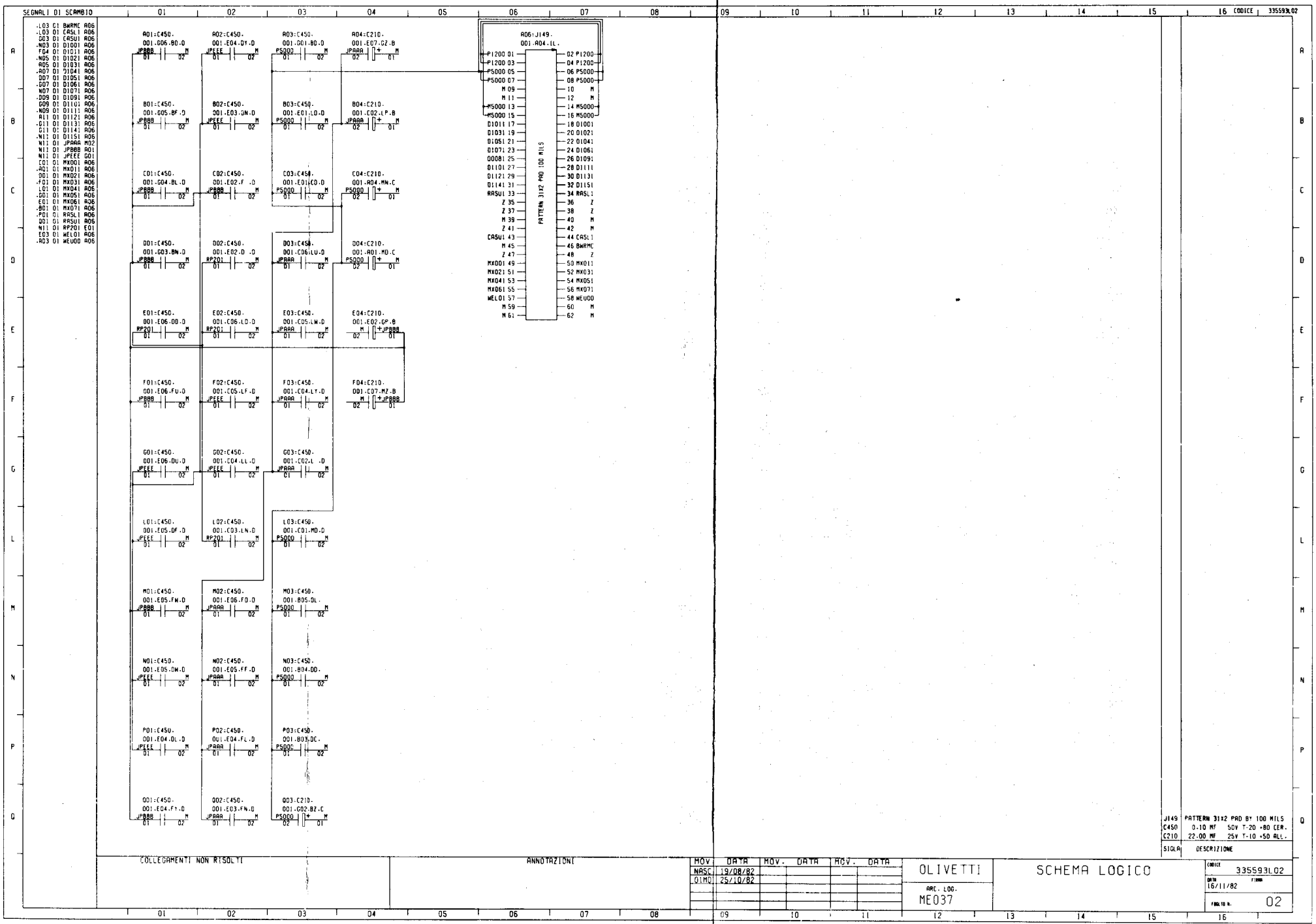
167003 Y		0001	TARGHETTA DATI PIASTRA				
339028 C		0001	CIRCUITO STAMPATO				
4865300 L	NEV2	1	74S00	D14	4 NAND 2I		
4865304 J	NEV1	4	74S04	D14	6 INVER		
4870920 E	MSVN	16	4116-2	D16	RAM 16384x1 DIN		
4869225 B	KRR2	4	INLIO RETE RES-T-S SX		33 OHM		
		J149	1	PATTERN 3142 PRD BY 100 MILS			
5070709 A	C450	35	0.10 MF	50V T-20 +80 CER.			
5053607 M	C210	7	22.00 MF	25V T-10 +50 ALL.			

CODICE	RIF.	Q.TA	DESCRIZIONE	CODICE	RIF.	Q.TA	DESCRIZIONE

OLIVETTI — COMPLESSIVO VIMO PIASTRA 001 ME037 — N. DISEGNO 335593L

ARCHIVIO LOGICO ME037	PER XP1000		MOV.	DATA	MOV.	DATA	
SOSTITUISCE IL		INCA	19/08/82			NPM	
SOSTITUITO DA		NASC	25/10/82			DATA 16/11/82	
						SCALA 1:1	CODICE 335593L

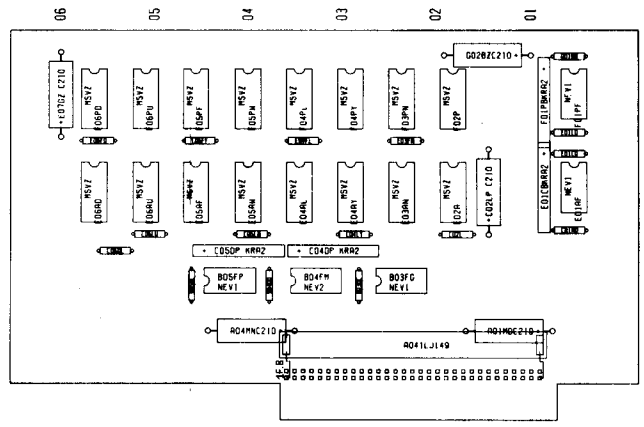




B03DC-C450
B04DD-C450
B05DL-C450
C01MD-C450
C02L -C450
C04LY-C450
C05LN-C450
C06DL-R07F
C06LU-C450
C01CD-C450
E01LD-C450
E03FN-C450
E04FL-C450
E05FF-C450
E06FD-C450
G0190-C450

CODICE 335594M

335594M01	0001	SCHEMA LOGICO
335594M02	0001	SCHEMA LOGICO
335594M03	0001	STIP
335594M04	0001	STAR
335594M05	0001	CAPO

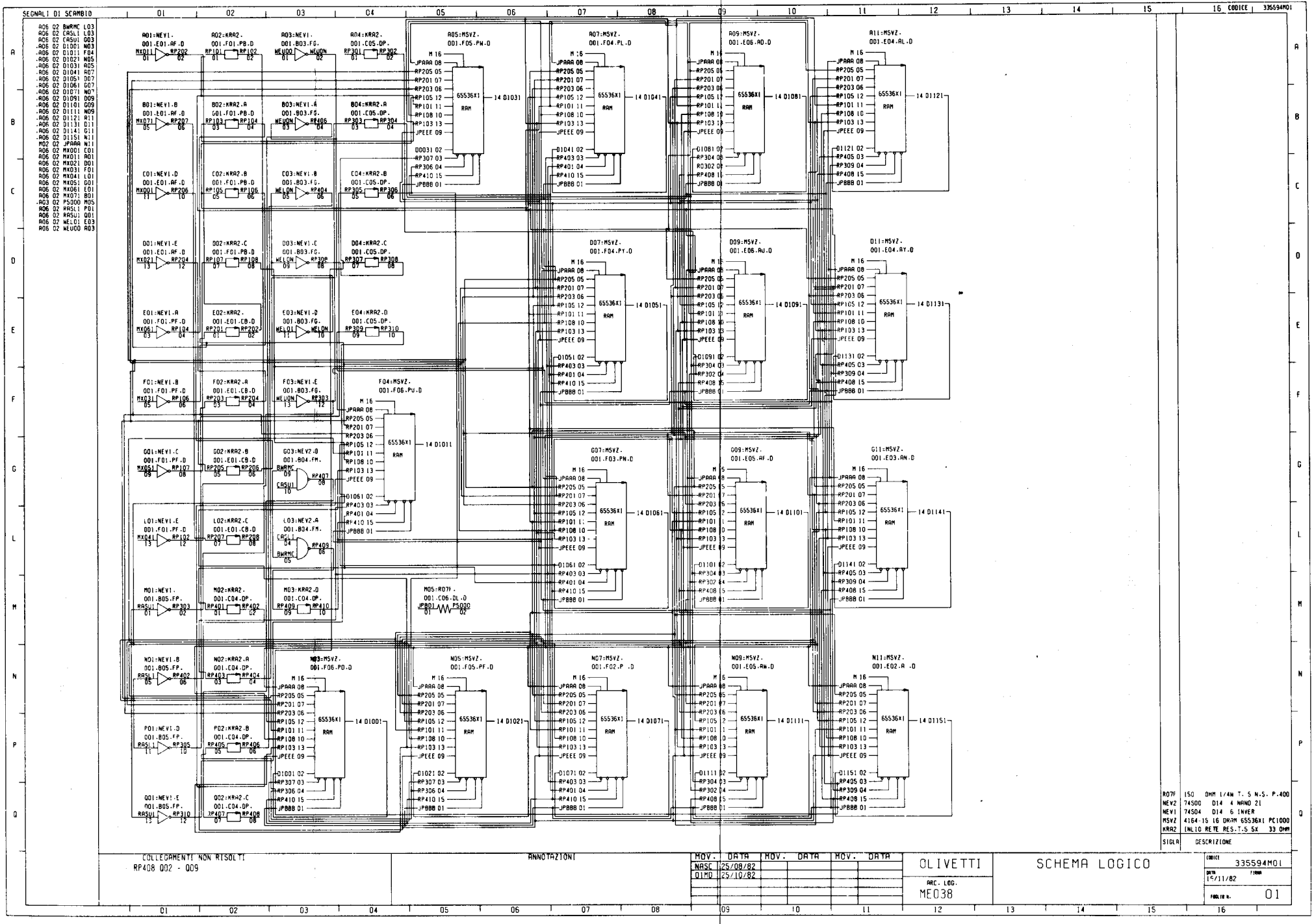


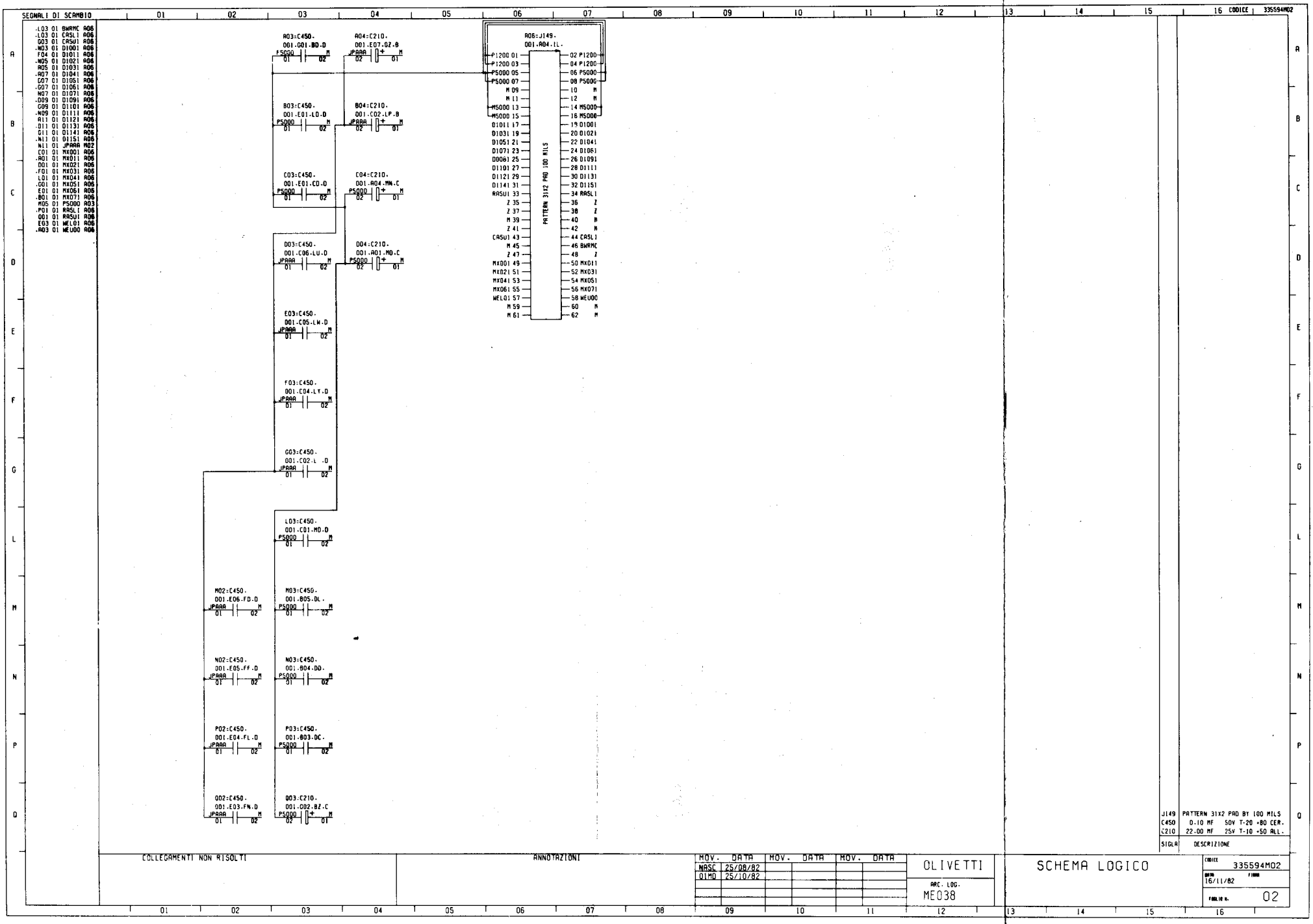
167003 Y		0001	TRASMETTR DATI PIASTRA	
339020 C		0001	CIRCUITO STAMPATO	
4865300 L	NEV2	1	74S00 DI4 4 NAND 2I	
4865304 J	NEV1	4	74S04 DI4 6 INVER	
4870941 H	M5V2	16	4164-15 16 DRAM 65536X1 PC1000	
4869225 B	KRA2	4	INL10 RETE RES.T-S SX 33 OHM	
4923231 P	R07F	1	150 OHM 1/4W T. 5 N.S. P.400	
	J149	1	PATTERN 31X2 PAD BY 100 MILS	
5070709 A	C450	15	0.10 MF 50V T-20 +80 CER.	
5053607 W	C210	5	22.00 MF 25V T-10 +50 ALL.	

CODICE	RIF.	Q.TA	DESCRIZIONE

CODICE	RIF.	Q.TA	DESCRIZIONE

OLIVETTI	COMPLESSIVO VIMO PIASTRA 001 ME038					N. DISEGNO 335594M	
ARCHIVIO LOGICO ME038	PER XP1000	MOV.	DATA	MOV.	DATA		
SOSTITUISCE IL		INCA	25/08/82			NPM	
SOSTITUITO DA		NASC	25/10/82			DATA 16/11/82	
						SCALA 1:1	CODICE 335594M

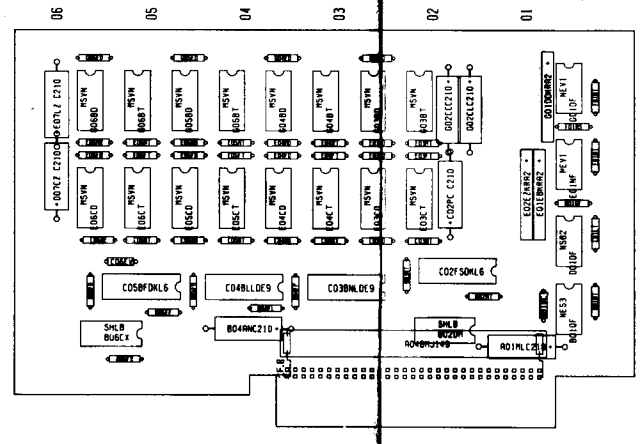




A06FX-C450
B01DC-R49R
B01DT-C450
B02MT-C450
B03MT-C450
B04FL-C450
B04FP-C450
B05EF-C450
B05FM-C450
B06FG-C450
C01LT-C450
C03ND-C450
C03NT-C450
C04ND-C450
C04NT-C450
C05ND-C450
C05NT-C450
C06EV-R49R
C06NE-C450
C06NT-C450
D01GF-C450
E01BT-C450
E03FD-C450
E03FT-C450
E03MD-C450
E03MT-C450
E04FD-C450
E04FT-C450
E04MD-C450
E04MT-C450
E05FD-C450
E05FT-C450
E05MD-C450
E05MT-C450
E06FD-C450
E06FT-C450
E06MD-C450
E06MT-C450
F01RS-C450
F01DT-C450
G03ED-C450
G04ED-C450
G05ED-C450
G06ED-C450

CODICE 335928T

335928TD1	0001	SCHEMA LOGICO
335928TD2	0001	SCHEMA LOGICO
335928TD4	0001	STAR
335928TD3	0001	STIP
335928TD5	0001	CAPO

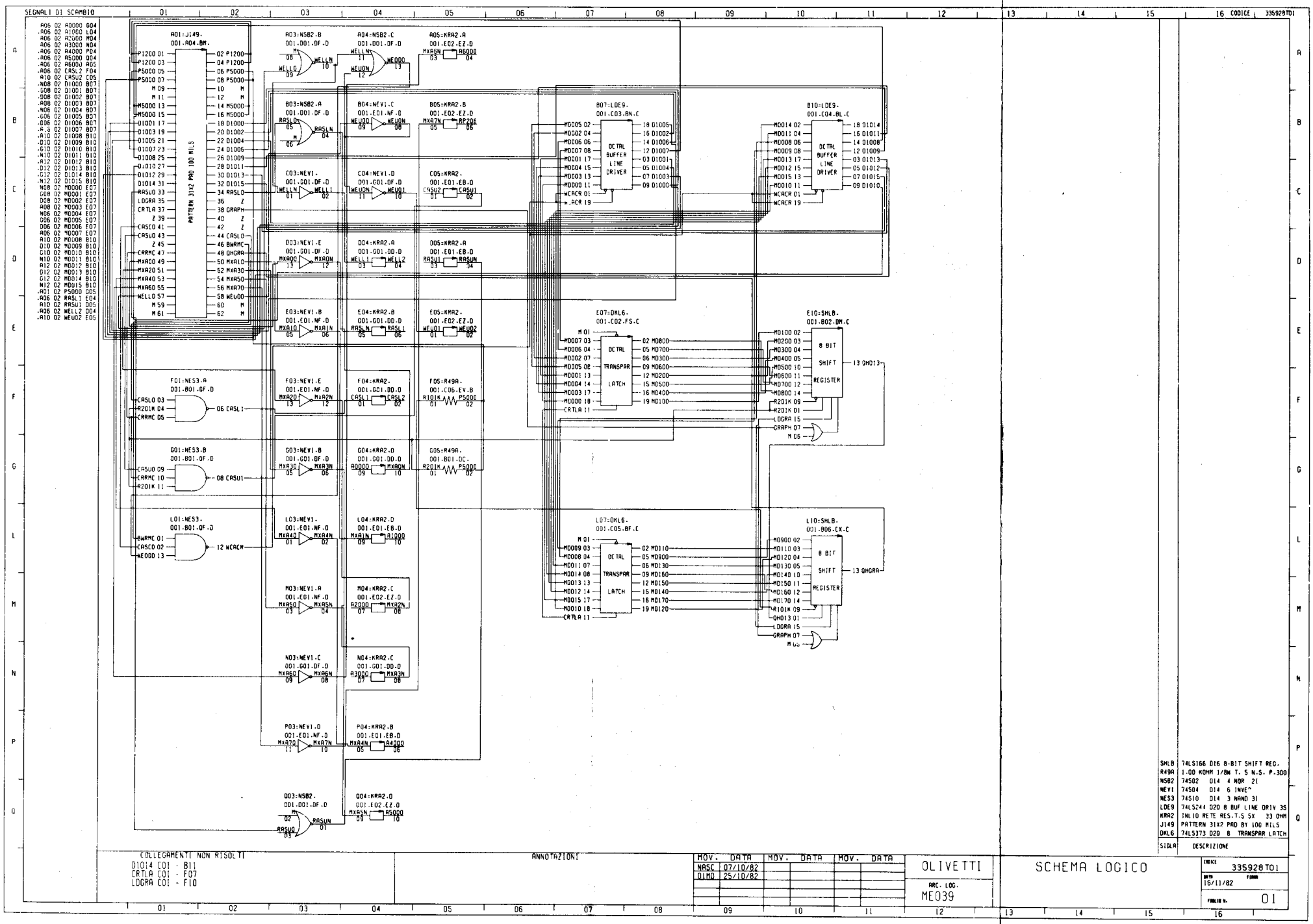


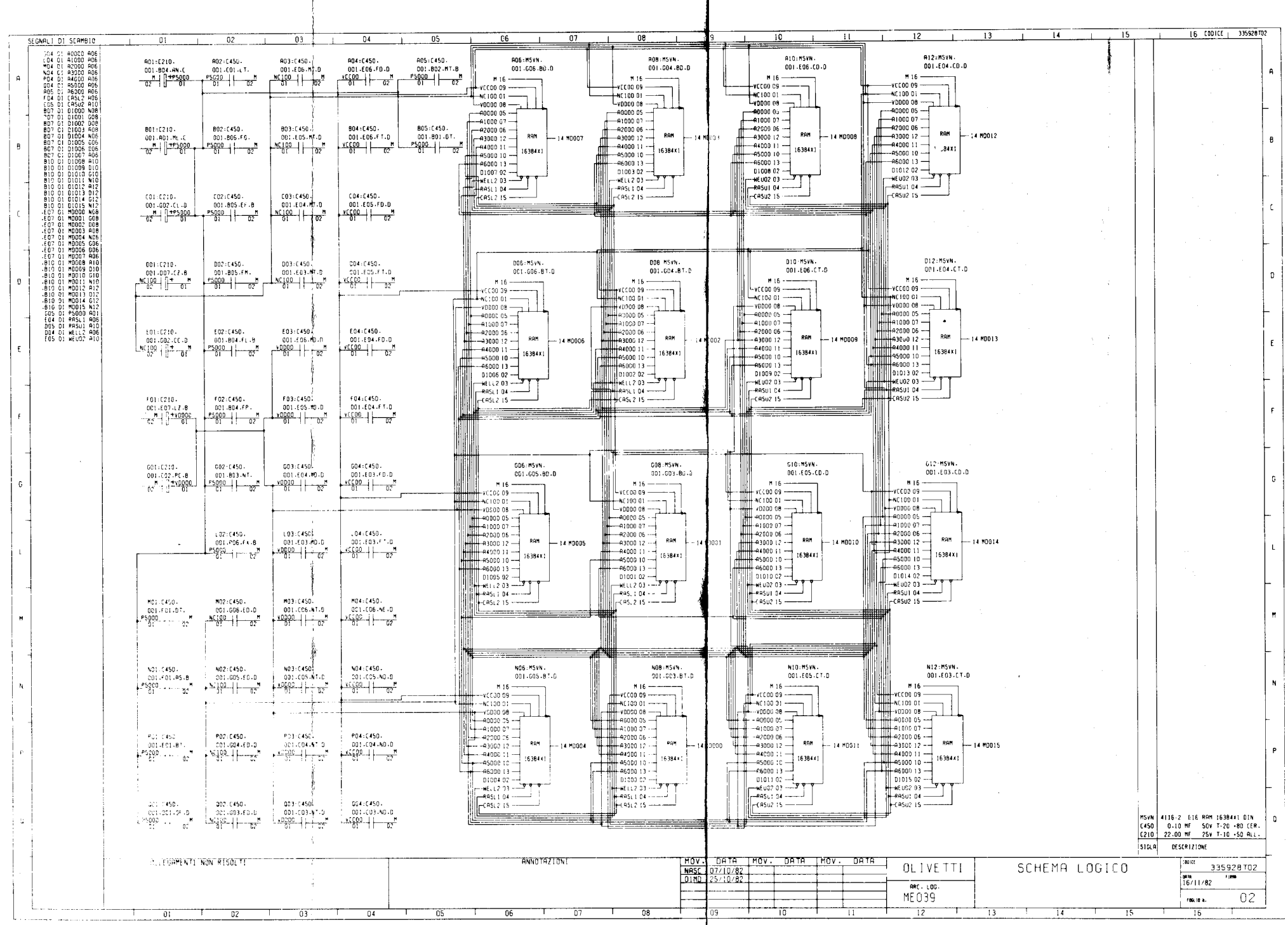
167003 Y		0001		TARGHETTA DATI PIASTRA
339106 G		0001		CIRCUITO STAMPATO
4867010 U	SHLB	2	74LS166	D16 8-BIT SHIFT REG.
4865304 J	NEV1	2	74S04	D14 6 INVER
4865315 B	NES3	1	74S10	D14 3 NAND 3I
4866294 Z	NSB2	1	74S02	D14 4 NOR 2I
4870920 E	MSVN	16	4116-2	D16 RAM 16384X1 DIN
4863455 Y	LDE9	2	74LS244	D20 8 BUF LINE DRIV 3S
4869225 B	KRA2	3	INL10	RETE RES.T.5 5% 33 OHM
4859423 V	DKL6	2	74LS373	D20 8 TRANSPAR LATCH
4900689 F	R49R	2		1.00 KOHM 1/8W T. 5 N.S. P.300
			J149	1 PATTERN 31X2 PAD BY 100 MILS
5070709 A	C450	42		0.10 MF 50V T-20 +80 CER.
5053607 W	C210	7		22.00 MF 25V T-10 +50 ALL.

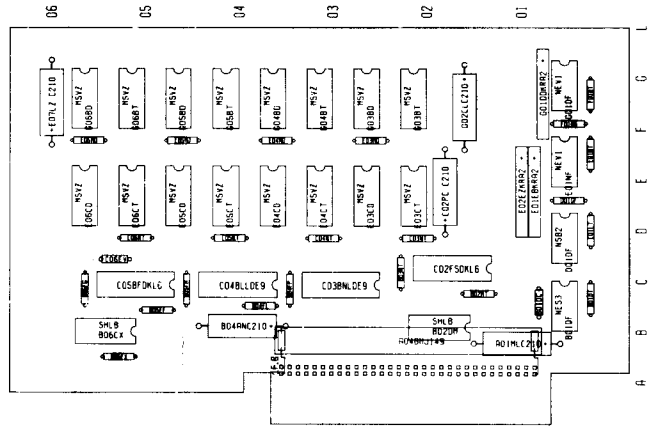
CODICE	RIF.	Q.TA	DESCRIZIONE	CODICE	RIF.	Q.TA	DESCRIZIONE

OLIVETTI — COMPLESSIVO VIMO PIASTRA 001 ME039 — N. DISEGNO 335928T

ARCHIVIO LOGICO ME039	PER XP1000	MOV.	DATA	MOV.	DATA
SOSTITUISCE IL		INCA	07/10/82		
SOSTITUITO DA		NASC	25/10/82		
				NPM	
				DATA 16/11/82	
				SCALA 1:1	CODICE 335928T







CODICE	335929U

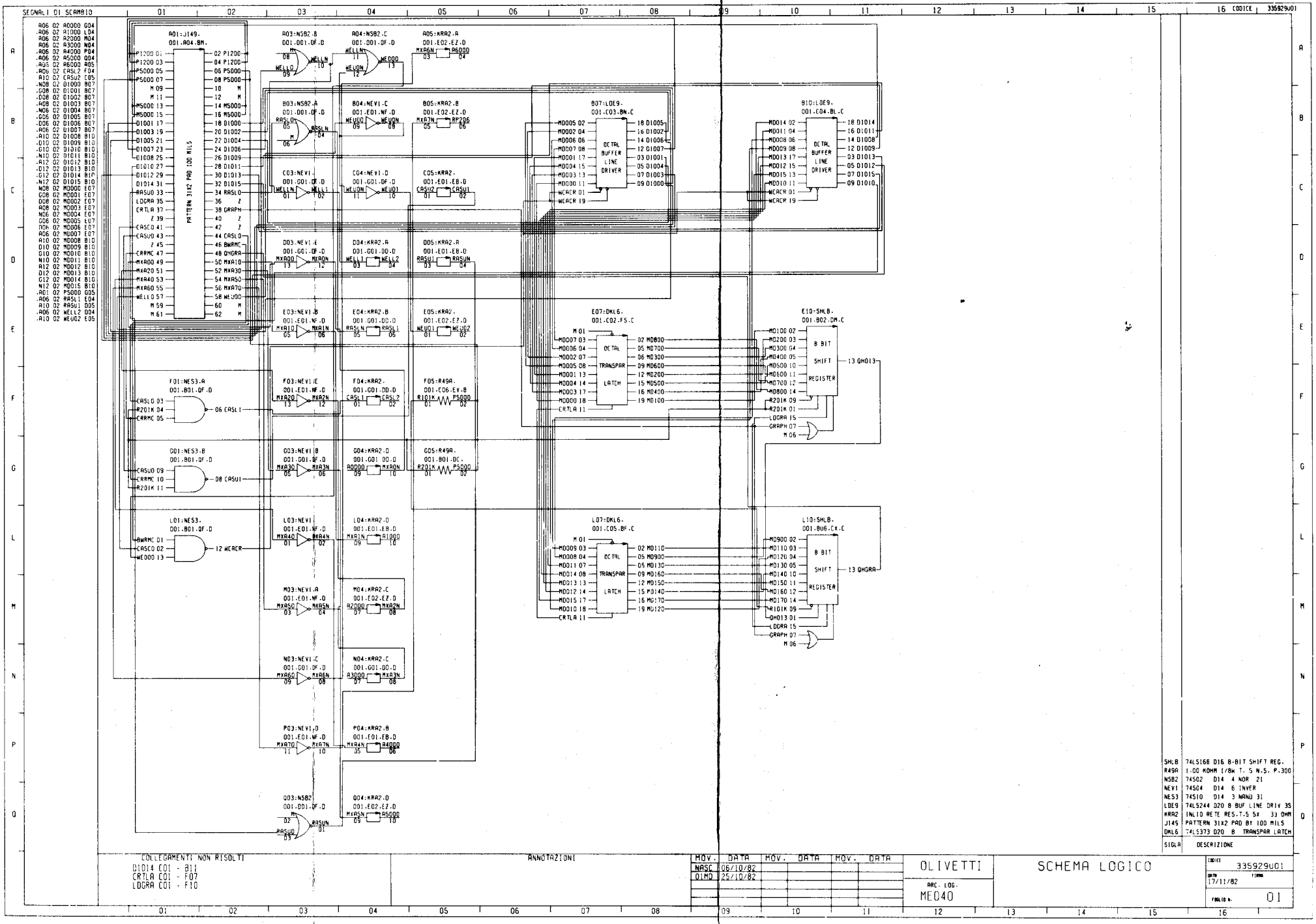
335929U01	0001	SCHEMA LOGICO
335929U02	0001	SCHEMA LOGICO
335929U04	0001	STAR
335929U03	0001	STIP
335929U05	0001	CAPO

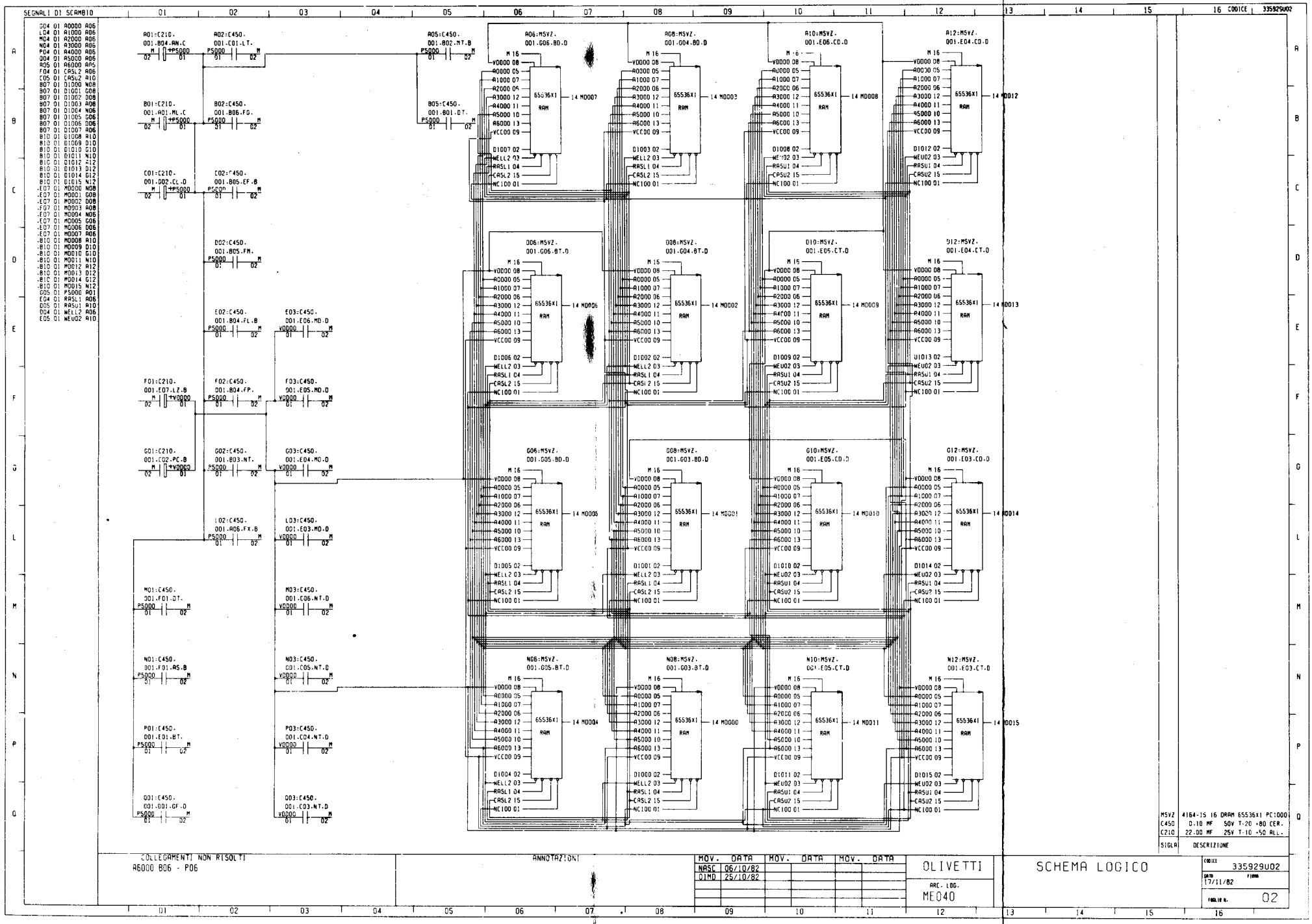
167003 Y		0001	TRASMETTR DATI PIASTRA	
339106 G		0001	CIRCUITO STAMPATO	
4867010 U	SMLB	2	74LS166 D16 8-BIT SHIFT REG.	
4865304 J	NEV1	2	74S04 D14 6 INVER	
4865315 B	NE53	1	74S10 D14 3 NAND 3I	
4866294 Z	NS82	1	74S02 D14 4 NOR 2I	
4870941 M	MSV2	16	4164-15 16 DRAM 65536X1 PC1000	
4863455 Y	LDE9	2	74LS244 D20 8 BUF LINE DRIV 3S	
4869225 B	KRA2	3	INLIO RETE RES.T-5 5% 33 OHM	
4859423 V	DML6	2	74LS373 D20 8 TRANSPAR LATCH	
4900689 F	R49A	2	1.00 KOHM 1/8W T. 5 N.S. P.300	
	J149	1	PATTERN 31X2 PAD BY 100 MILS	
5070709 R	C45D	22	0.10 MF 50V T 20 +80 CER.	
5053607 W	C21D	5	22.00 MF 25V T-10 +50 ALL.	

CODICE	RIF.	Q.TA	DESCRIZIONE
R06FX	C45D		
B01DC	R49A		
B01DT	C45D		
B02MT	C45D		
B03NT	C45D		
B04FL	C45D		
B04FP	C45D		
B05EF	C45D		
B05FM	C45D		
B06FG	C45D		
C01LT	C45D		
C03NT	C45D		
C04NT	C45D		
C05NT	C45D		
L06EW	R49A		
C06NT	C45D		
D01CF	C45D		
E01BT	C45D		
E03MD	C45D		
E04MD	C45D		
E05MD	C45D		
E06MD	C45D		
F01AS	C45D		
F01BT	C45D		

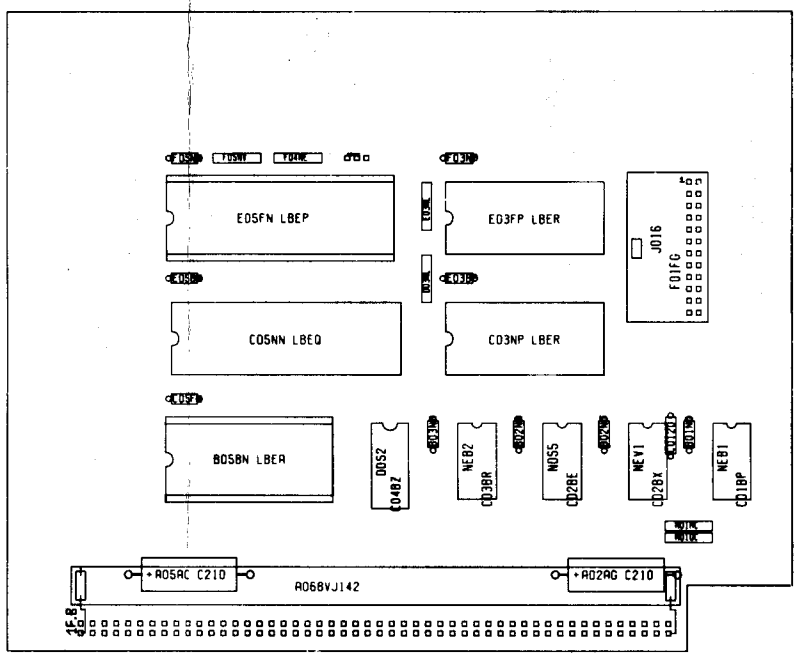
CODICE	RIF.	Q.TA	DESCRIZIONE
5070709 R	C45D	22	0.10 MF 50V T 20 +80 CER.
5053607 W	C21D	5	22.00 MF 25V T-10 +50 ALL.

OLIVETTI	COMPLESSIVO VIMD PIASTRA 001 ME040					N. DISEGNO 335929U	
ARCHIVIO LOGICO ME040	PER XP1000	MOV.	DATA	MOV.	DATA		
SOSTITUISCE IL		INCR	06/10/82			WPM	
SOSTITUITO DA		NASC	25/10/82			DATA 17/11/82	
						SCALA 1:1	CODICE 335929U





A01GC-R89E
A01ME-R89E
B01NG-C640
B02NA-C640
B02NT-C640
B03NM-C640
C012D-R51A
C05FN-C640
D03NL-R21F
E03BP-C640
E03NL-R21F
E05BN-C640
F03NP-C640
F04NE-R21F
F04NV-P011
F05NN-C640
F05NY-R21F

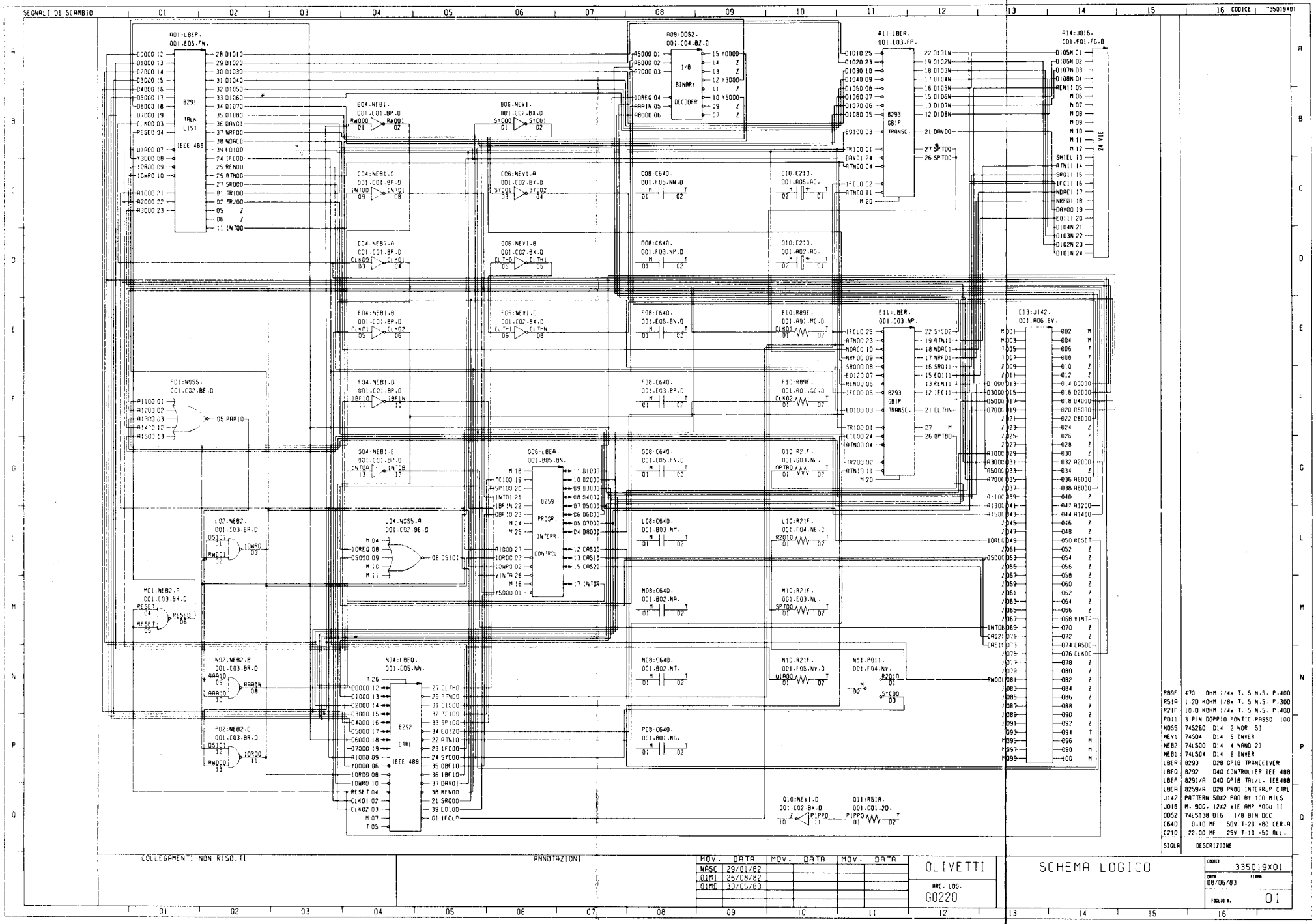


CODICE 335019X

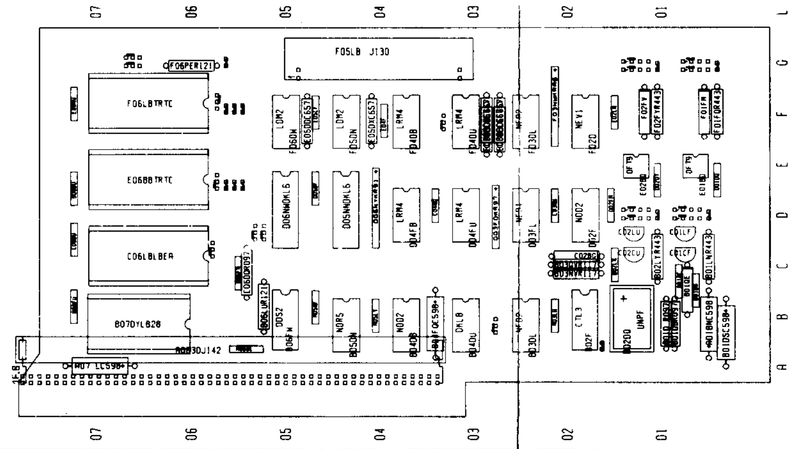
335019X06 0001 SCHEMA INTERRUZIONI E FILATURE
335019X01 0001 SCHEMA LOGICO
NOTA:
LA RESISTENZA R51A DA 1.2K 1/8 WATT.VIENE MONTATA TRA IL PIN 11 E IL PIN 14 DEL COMPONENTE 74S04 IN POSIZIONE C02BX.

CODICE	RIF.	Q.TA	DESCRIZIONE
167003 Y	ZTAR	0001	TARGHETTA DATI PIASTRA
339026 S		0001	CIRCUITO STAMPATO
4866299 W	N0S5	1	74S260 D14 2 NOR 5I
4865304 J	NEV1	1	74S04 D14 6 INVER
4866280 S	NEB2	1	74LS00 D14 4 NAND 2I
4866303 H	NEB1	1	74LS04 D14 6 INVER
4863026 A	LBER	2	8293 D28 GPIB TRANCEIVER
4863025 W	LBEQ	1	8292 D40 CONTROLLER IEE 488
5775034 W	LBEP	1	***** SOCKET DIL 40-600
4863024 S	LBEP	1	8291/A D40 GPIB TAL/L. IEE488
5775028 W	LBEA	1	***** SOCKET DIL 28-600
4863862 V	LBEA	1	8259/A D28 PROG INTERRUP CTRL
4864239 G	0DS2	1	74LS138 D16 1/8 BIN DEC
4900693 N	R51A	1	1.20 KOHM 1/8W T. 5 N.S. P.300
4925058 M	R21F	4	10.0 KOHM 1/4W T. 5 N.S. P.400
4923710 W	R89E	2	470 OHM 1/4W T. 5 N.S. P.400
5785920 S	P011	1	***** BLOCCHETTO 3 VIE MINIVIP
5775100 S	P011	1	3 PIN DOPPIO PONTIC.PASSO 100
5785786 Z	J016	1	M. 90G. 12X2 VIE AMP-MODU II
	J142	1	PATTERN 50X2 PAD BY 100 MILS
5070709 A	C640	9	0.10 MF 50V T-20 +80 CER.A
5053607 W	C210	2	22.00 MF 25V T-10 +50 ALL.

OLIVETTI		COMPLESSIVO VIMO PIASTRA 001 C0220						N. DISEGNO 335019X
ARCHIVIO LOGICO C0220		PER XP1000	MOV.	DATA	MOV.	DATA		
SOSTITUISCE IL			INCA	28/01/82			NPM	
SOSTITUITO DA			NASC	29/01/82				
			01M1	26/08/82			DATA 08/06/83	
			01M0	30/05/83			SCALA 1:1	CODICE 335019X



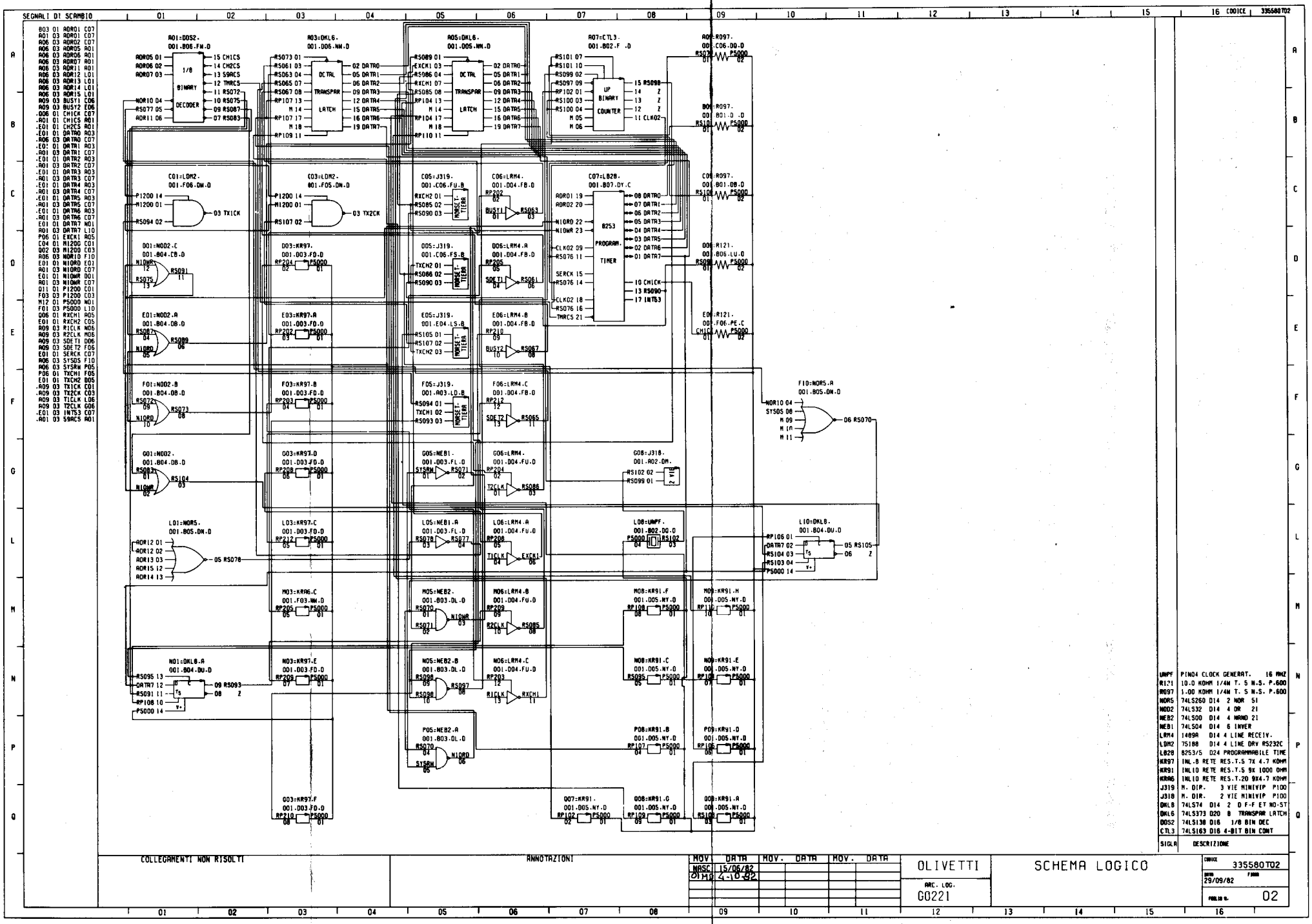
A02DG-J318
A03LD-J319
A03LW-C450
A05LY-C450
A05NF-C450
A0?DL-C450
B?1BG-R14F
B01QC-R10F
B01QE-D170
B02LN-R14F
B06FN-C450
B08FU-C450
C01CF-Q114
C01LF-Q114
C01PN-J318
C02BG-D170
C02CU-Q114
C02LU-Q114
C02PY-J318
C03NW-C450
C04NQ-C450
C06FS-J319
C06FU-J319
C08BU-C450
D01DQ-R14F
D02DY-R14F
D02FM-R10F
D05BF-C450
D06FE-J319
D06FG-J318
D06FM-J318
D06FP-J318
D08BU-C450
E02LN-C450
E04F -C450
E04LS-J319
E05LF-C450
E06QG-J318
E06QM-J318
E06QP-J318
E08NU-C450
F01FM-D170
F01NQ-J318
F02FV-D170
F02NY-J318
F06DE-J319
F06PG-J318
F07PF-J319
G07AF-J319
C01 -J158
C02 -J158
C06 -J319
D01 -J158
D02 -J158
F01 -J158
F01 -J158
F02 -J158
F02 -J158

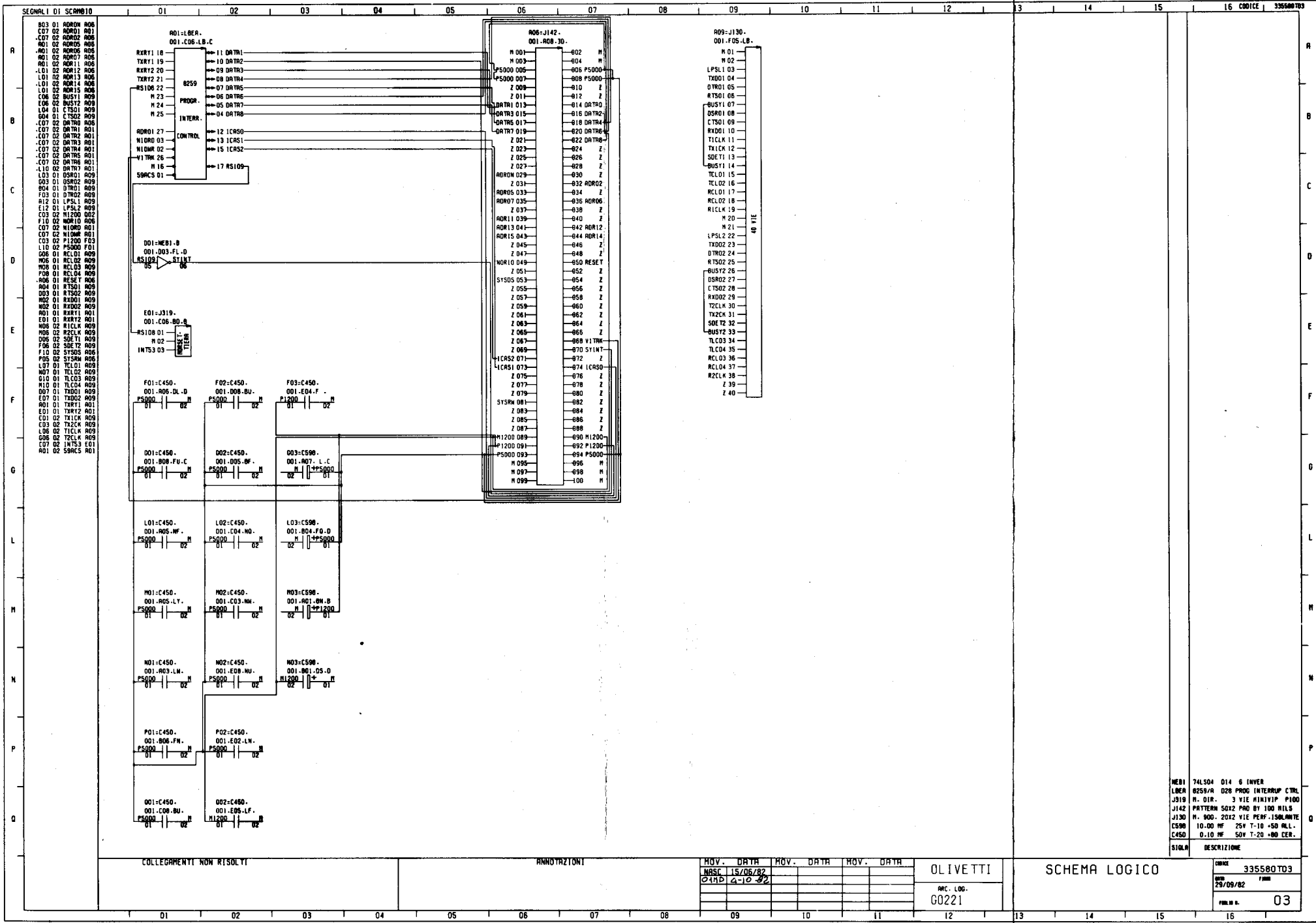


			CODICE 335580T
335580TD1		0001	SCHEMA LOGICO
335580TD2		0001	SCHEMA LOGICO
335580TD3		0001	SCHEMA LOGICO
335580TD4			STAR
335580TD5			STIP
335580TD6			CAPO
335580TD7			PONTICELLATURE
5775101 T		0023	PIN JUMPER
167003 Y			TARGHETTA DATI PIASTRA
339027 T			CIRCUITO STAMPATO
5775028 W	TRTC	2	***** SOCKET DIL 28-600
4863016 H	TRTC	2	8251/A D28 SYNC/ASYNC R/T
4865304 J	NEV1	1	74S04 D14 6 INVER
4866298 S	NOR5	1	74LS260 D14 2 NOR 5I
4866287 C	NOD2	2	74LS32 D14 4 OR 2I
4866269 K	NFB2	1	74LS08 D14 4 AND 2I
4866280 S	NEB2	1	74LS00 D14 4 NAND 2I
4866303 H	NEB1	1	74LS04 D14 6 INVER
4881515 Y	UNPF	1	PIN04 CLOCK GENERAT. 16 MHZ
4863404 B	LRM4	4	1489A D14 4 LINE RECEIV.
4863402 J	LDM2	2	75188 D14 4 LINE DRV RS232C
5775023 G	LB28	1	***** SOCKET DIL 24-600
4863655 U	LB28	1	8253/5 D24 PROGRAMMABILE TIME
5775028 W	LBEA	1	***** SOCKET DIL 28-600
4863862 V	LBEA	1	8259/A D28 PROG INTERRUP CTRL
4869255 E	KR97	1	INL.8 RETE RES.T.5 7X 4.7 KOHM
4869229 C	KR91	1	INL10 RETE RES.T.5 9X 1000 OHM
4869242 Q	KRA6	1	INL10 RETE RES.T.20 9X4.7 KOHM
4859429 P	DKL8	1	74LS74 D14 2 D F-F ET NO-ST
4859423 V	DKL6	2	74LS373 D20 8 TRANSPAR LATCH
4847979 M	OFT9	2	TIL117 D06 OPTICAL COUPL ISOL
4864239 G	DDS2	1	74LS138 D16 1/8 BIN DEC
4862278 P	CTL3	1	74LS163 D16 4-BIT BIN CONT
4925690 V	R14F	4	47.0 KOHM 1/4W T. 5 N.S. P.400
4925058 M	R121	2	10.0 KOHM 1/4W T. 5 N.S. P.600
4924849 C	R117	2	6.80 KOHM 1/4W T. 5 N.S. P.600
4924698 Y	R10F	2	4.70 KOHM 1/4W T. 5 N.S. P.400
4924070 L	R097	3	1.00 KOHM 1/4W T. 5 N.S. P.600
4933685 E	R443	4	470. OHM 1/2W T. 2 A.S. P.600
4849690 W	Q114	4	2N3904 TO92 NPN 200MA 40V SI
5787286 X	J130	1	M. 90G. 20X2 VIE PERF.ISOLANTE
5785920 S	J319	9	M. DIR. 3 VIE MINIVIP P100
5785930 T	J318	12	M. DIR. 2 VIE MINIVIP P100
5785931 U	J158	8	M. DIR. 4.VIE MINIVIP
	J142	1	PATTERN 50X2 PAD BY 100 MILS
4800146 S	D170	4	1N4448 75V .15A DIOD SIL-VEL
5037454 E	C598	4	10.00 MF 25V T-10 +50 ALL.
5070709 A	C450	15	0.10 MF 50V T-20 +80 CER.
5070597 J	C657	6	330 PF 50V T-20 +20 CER.
CODICE	RIF.	Q.TA	DESCRIZIONE

CODICE	RIF.	Q.TA	DESCRIZIONE

OLIVETTI	COMPLESSIVO VIMO PIASTRA 001 G0221					N. DISEGNO 335580T
ARCHIVIO LOGICO G0221	PER XP1000	MOV.	DATA	MOV.	DATA	
		INCA	15/06/82			
SOSTITUISCE IL		NASC	24/05/83			NPM
SOSTITUITO DA						DATA 26/05/83
						SCALA 1:1 / CODICE 335580T



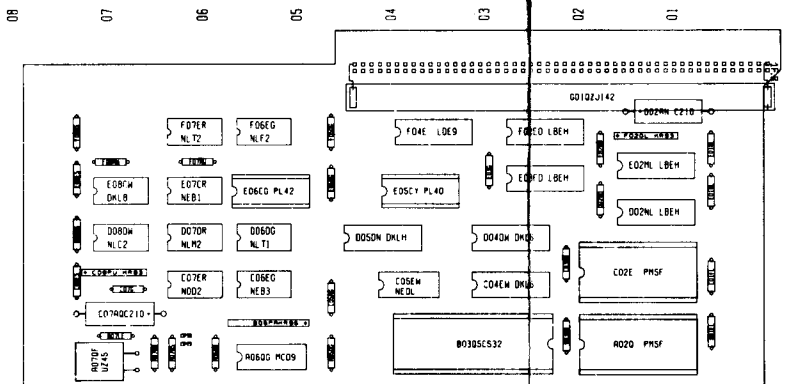


A05QG-C45D
A06QB-C45D
A07QN-R90E
A07QS-R90E
B01EL-C45D
B03QW-C45D
B07LE-R21F
C01FL-C45D
C03MW-C45D
C05AG-C45D
C07G -C45D
C08ES-C45D
D02GD-C45D
D08QS-C45D
F01BL-C45D
F01QL-C45D
F02QD-C45D
F03G -C45D
F05QG-C45D
F08ES-C45D
F0SQG-C45D
F07AU-C45D
F08AW-R97E
F08QS-C45D
B07 -J31B
B07 -J31B

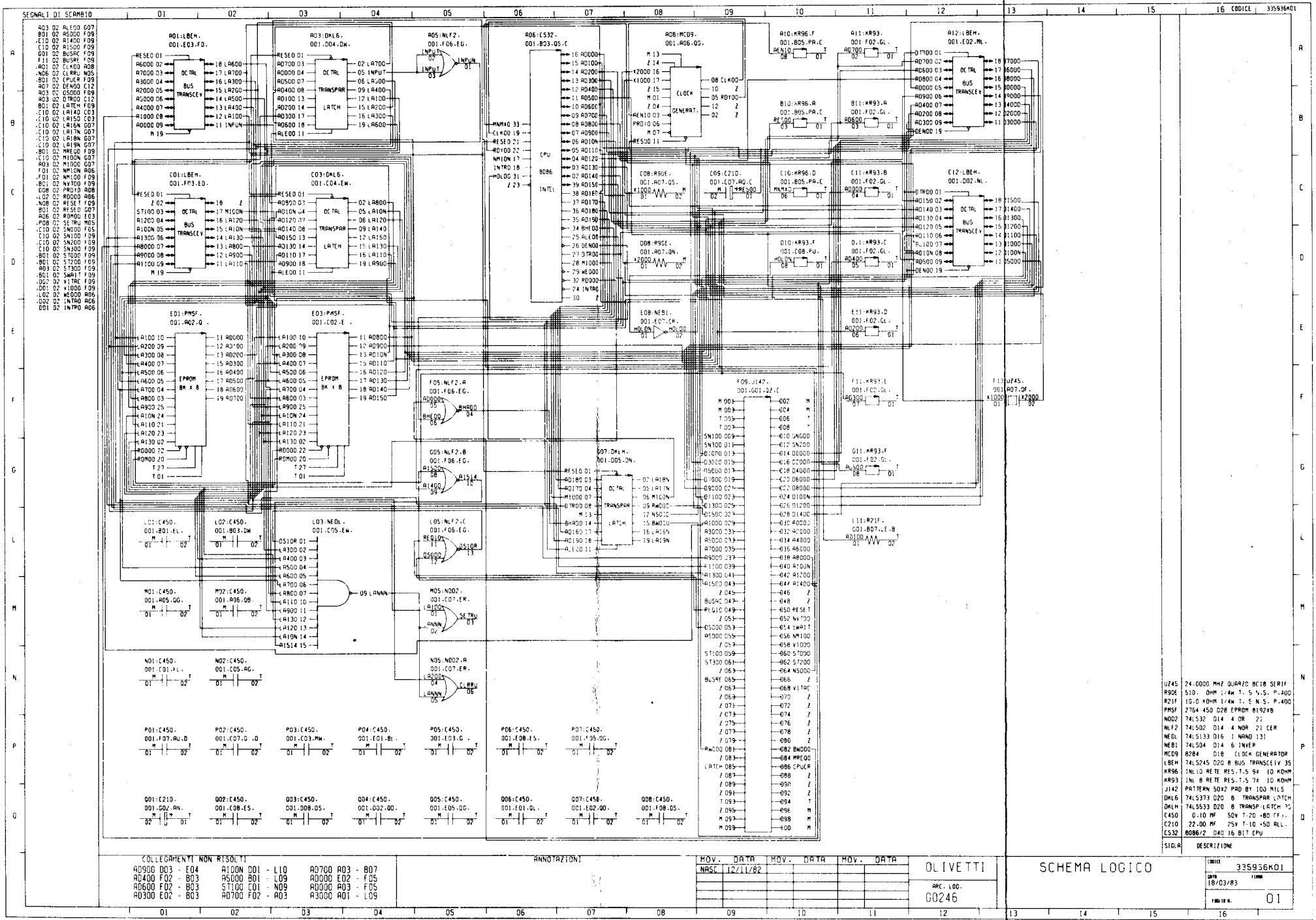
CODICE 335936K

335936K01		0001	SCHEMA LOGICO
335936K02		0001	SCHEMA LOGICO
335936K03		0001	STIP
335936K04		0001	STAR
335936K05		0001	CAPO

167003	Y	ZTAR	0001	TARGHETTA DATI PIASTRA
339109	K		0001	CIRCUITO STAMPATO
336233	T	PA69	0001	EPROM
336234	U	PA70	0001	EPROM
5775021	Y	PL42	1	***** SOCKET DIL 20-300
336590	W	PL42	1	P16R6 D20 RET-L P-U18 V2.1
5775021	Y	PL40	1	***** SOCKET DIL 20-300
336293	Y	PL40	1	P16L8 D20 RET-L. P U17 V 2.3
4866287	C	NOD2	1	74LS32 D14 4 OR 2I
4865363	P	NLT2	1	74LS132 D14 4 NAND 2I S-TRIG
4866315	P	NLT1	1	74LS14 D14 6 INVER S-TRIG
4865279	G	NLM2	1	74LS09 D14 4 AND 2I OC
4866292	G	NLF2	1	74LS02 D14 4 NOR 2I CER
4866276	X	NLC2	1	74LS00 D14 4 NAND 2I CER.
4865308	K	NEOL	1	74LS133 D16 1 NAND 13I
4866282	F	NEB3	1	74LS10 D14 3 NAND 3I
4866303	H	NEB1	1	74LS04 D14 6 INVER
5775028	W	PMSF	2	***** SOCKET DIL 28-600
4872640	W	PMSF	2	2764-450 D28 EPROM 8192X8
4863036	B	MC09	1	8284 D18 CLOCK GENERATOR
4863455	Y	LDE9	1	74LS244 D20 8 BUF LINE DRIV 3S
4863458	V	LBEH	4	74LS245 D20 8 BUS TRANSCEIV 3S
4869243	L	RR96	1	INL10 RETE RES.T.S 9X 10 KOHM
4869230	A	RR93	2	INL 8 RETE RES.T.S 7X 10 KOHM
4859429	P	DKL8	1	74LS74 D14 2 D F-F ET NO-ST
4859423	V	DKL6	2	74LS373 D20 8 TRANSPAR LATCH
4859436	T	DKLM	1	74LS533 D20 8 TRANSP-LATCH 3S
5775034	W	CS32	1	***** SOCKET DIL 40-600
4863047	G	CS32	1	8086/2 D40 16 BIT CPU
4875056	X	UZ4S	1	24.0000 MHZ QUARZO BC18 SERIF
4924070	L	R97E	1	1.00 KOHM 1/4W T. 5 N.S. P.400
4925058	M	R21F	1	10.0 KOHM 1/4W T. 5 N.S. P.400
4933736	F	R90E	2	510. OHM 1/4W T. 5 N.S. P.400
5705930	T	J31B	2	M. DIR. 2 VIE MINIVIP P10O
		J142	1	PATTERN 50X2 PAS BY 100 MILS
5070709	A	C450	20	0.10 MF 50V T-20 +80 CER.
5053607	W	C210	2	22.00 MF 25V T-10 +50 ALL.



CODICE	RIF.	Q.TA	DESCRIZIONE	CODICE	RIF.	Q.TA	DESCRIZIONE
OLIVETTI			COMPLESSIVO VIMO PIASTRA 001 G0246				N. DISEGNO 335936K
ARCHIVIO LOGICO G0246			PER XP1000	MOV.	DATA	MOV.	DATA
SOSTITUISCE IL				IMCA	12/11/82		
SOSTITUITO DA				MASC	01/12/82		
				DIM1	10/03/83		
							NPM
							DATA 15/03/83
							SCALA 1:1
							CODICE 335936K



COLLEGAMENTI NON RISOLTI			
AD900 D03 - E04	A100N D01 - L10	AD700 A03 - B07	
AD400 F02 - B03	A5000 B01 - L09	AD000 E02 - F05	
AD600 F02 - B03	ST100 C01 - N09	AD000 A03 - F05	
AD300 E02 - B03	AD700 F02 - A03	A3000 A01 - L09	

ANNOTAZIONI

MOV.	DATA	MOV.	DATA	MOV.	DATA
NASC	12/11/82				

OLIVETTI

ARC. LOG. G0246

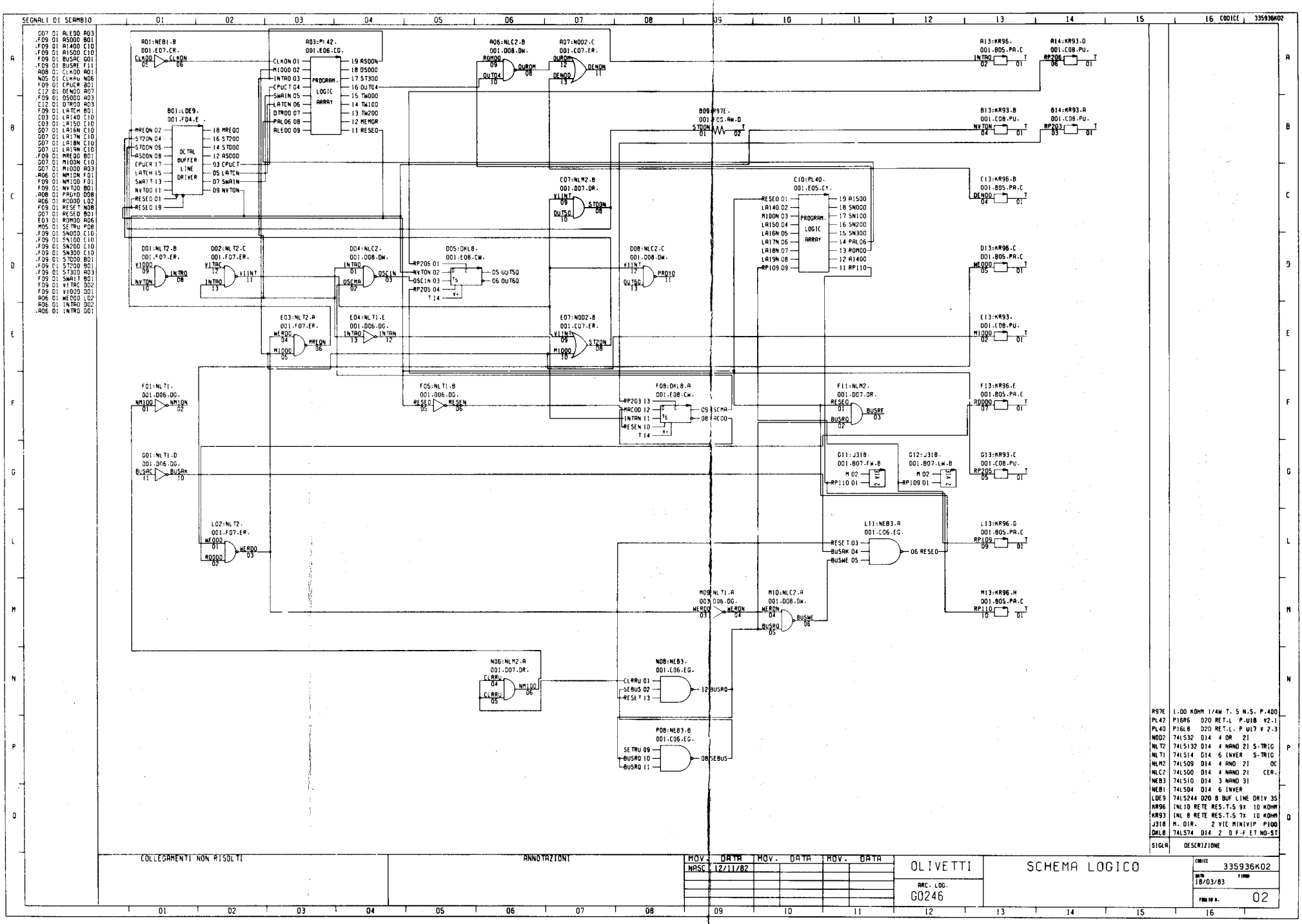
SCHEMA LOGICO

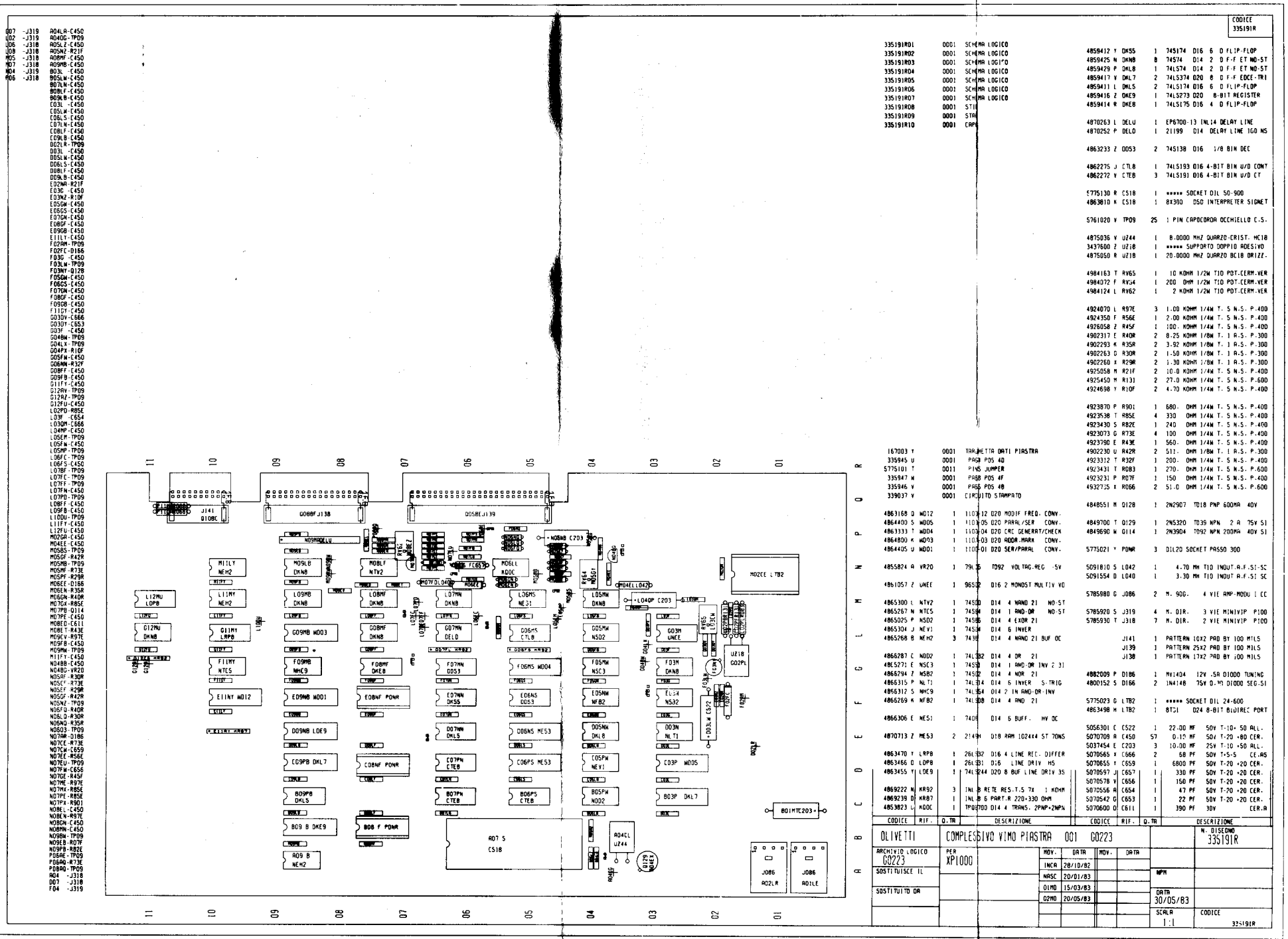
CODICE 335936K01

DATA 18/03/83

FOGLIO N. 01

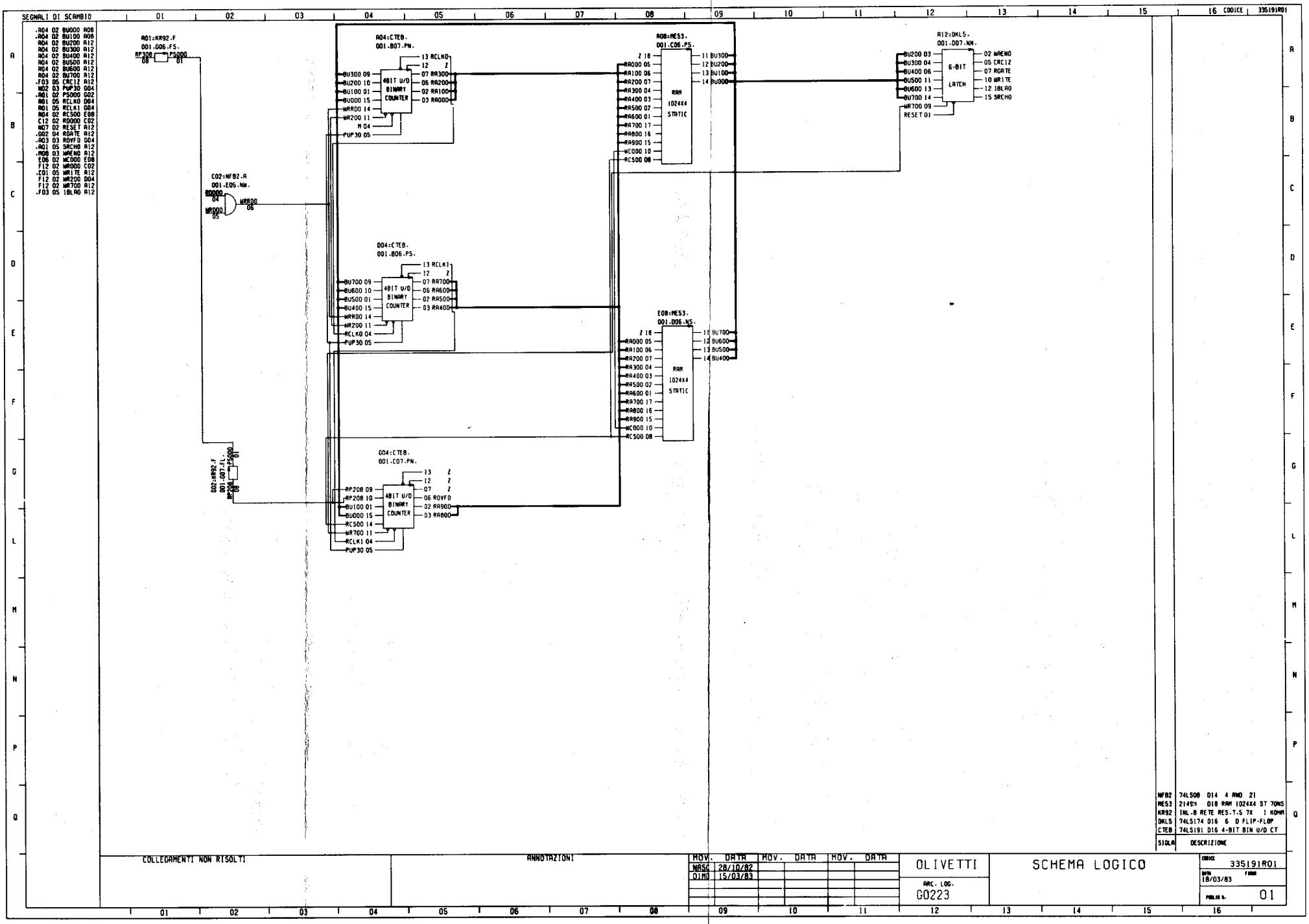
SIGLA	DESCRIZIONE
UZ45	24.0000 MHZ QUARZO BC18 SERIE
R5DE	510. OHM 1/4W T.5 %.S. P.400
R21F	10.0 KOHM 1/4W T.5 %.S. P.400
PMSF	2764 450 028 EPROM 8192X8
NOD2	74LS32 D14 4 OR 21
NLF2	74LS02 D14 4 NOR 21 CER
NEDL	74LS133 D16 1 NAND 131
NEB1	74LS04 D14 6 INVER
MCD9	8284 D18 CLOCK GENERATOR
LBEM	74LS245 D20 8 BUS TRANSCEIV 35
KR96	INL10 RETE RES.T.5 9X 10 KOHM
KR93	INL 8 RETE RES.T.5 7X 10 KOHM
J142	PATTERN SOX2 PAD BY 100 MILS
DML6	74LS373 D20 8 TRANSPAR LATCH
DKLM	74LS533 D20 8 TRANSP-LATCH 3S
C450	0.10 MF 50V T-20 -80 FF+.
C210	22.00 MF 25V T-10 +50 ALL.
CS32	8086/2 D40 16 BIT CPU

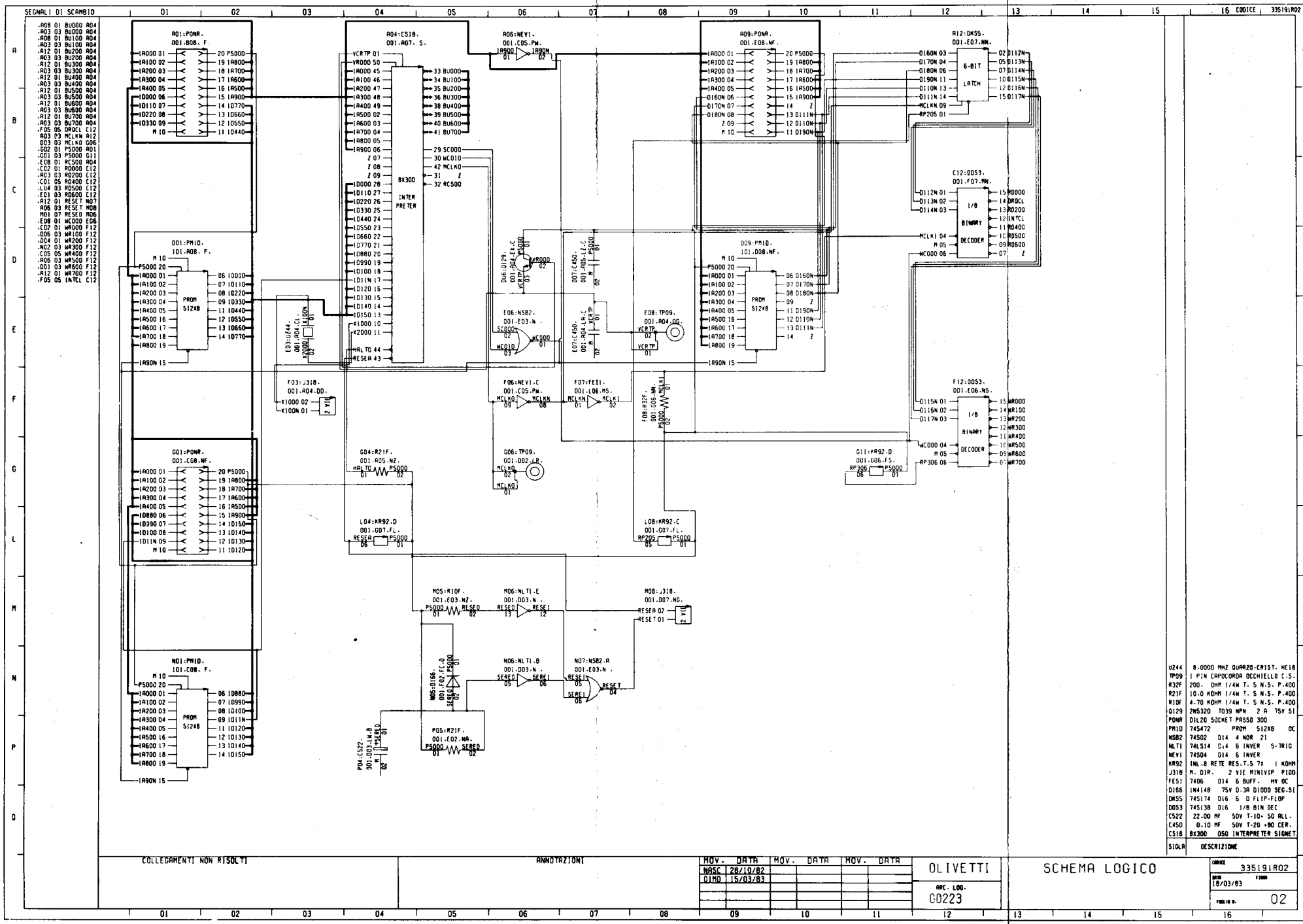


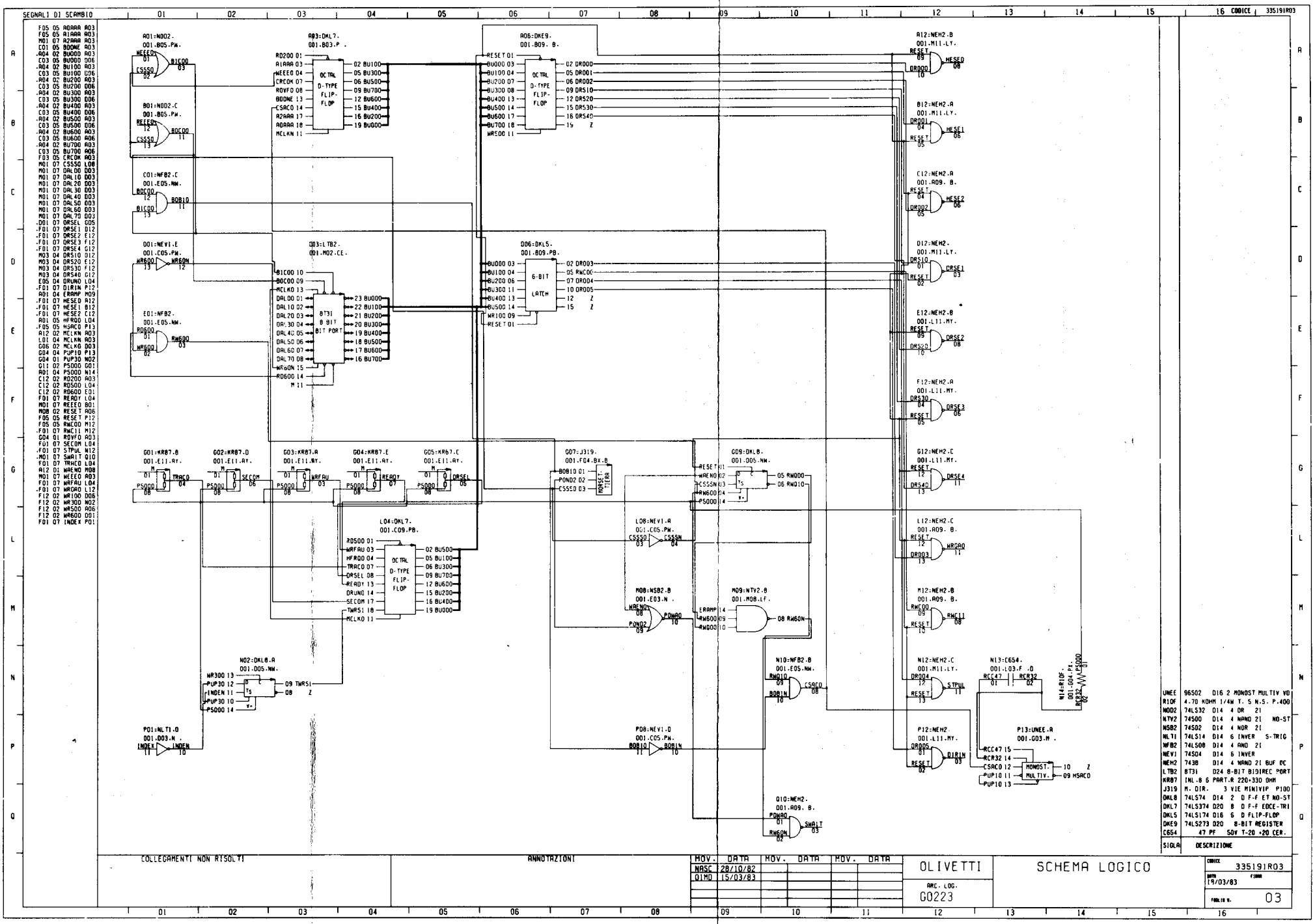


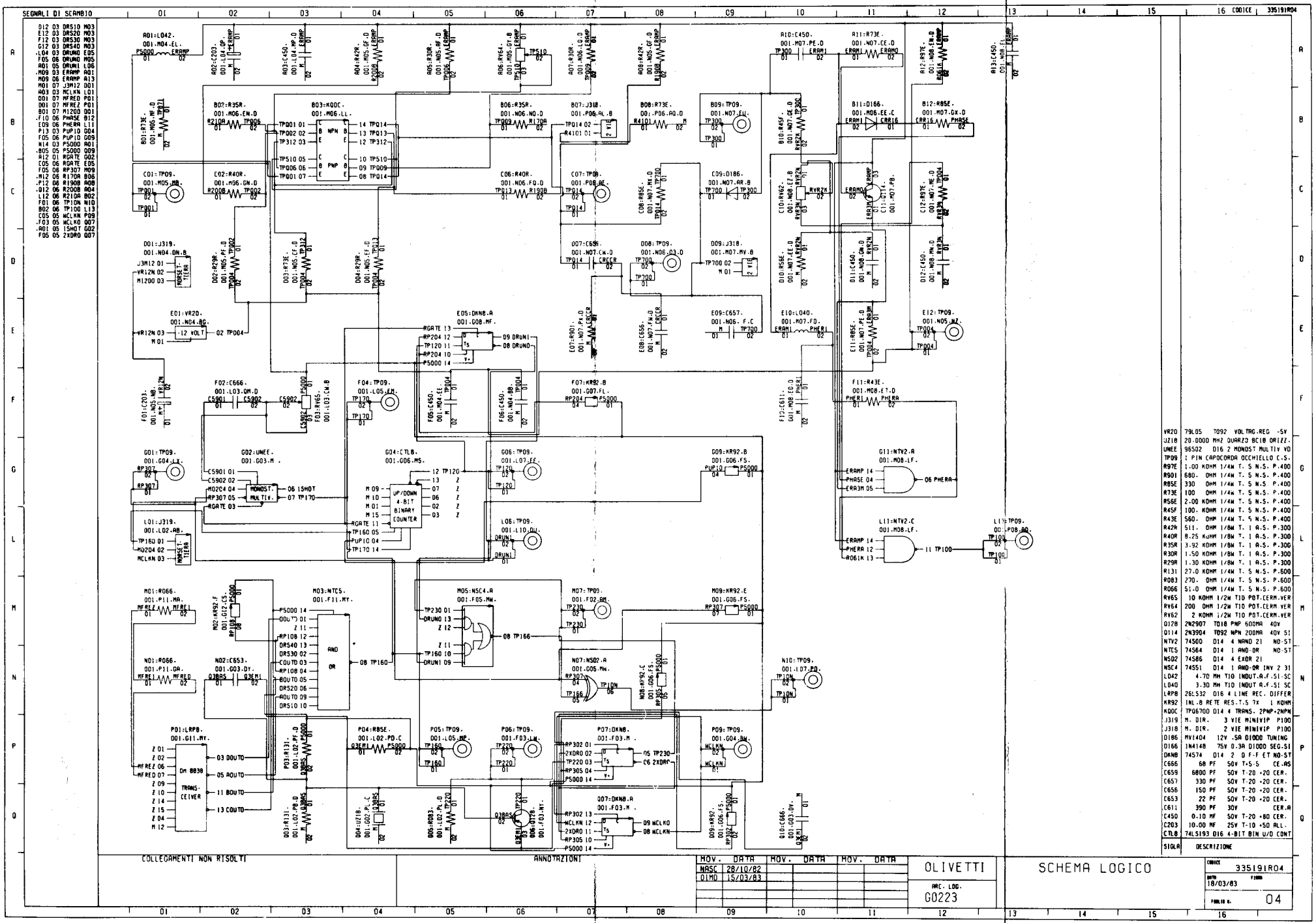
CODICE	RIF.	Q.TA	DESCRIZIONE
335191R01		0001	SCHEMA LOGICO
335191R02		0001	SCHEMA LOGICO
335191R03		0001	SCHEMA LOGICO
335191R04		0001	SCHEMA LOGICO
335191R05		0001	SCHEMA LOGICO
335191R06		0001	SCHEMA LOGICO
335191R07		0001	SCHEMA LOGICO
335191R08		0001	STI
335191R09		0001	STR
335191R10		0001	CAP
1670037 Y		0001	TARATURA DATI PIASTRA
335945 U		0001	PASS POS 40
5775101 T		0011	PINS JUMPER
335947 W		0001	PASS POS 4F
335946 V		0001	PASS POS 4B
339037 Y		0001	CIRCUITO STAMPATO
4863168 Q	WD12	1	11D1-12 D20 MODIF FREQ. CONV.
4864400 S	WD05	1	11D1-05 D20 PARAL/SER CONV.
4863333 T	WD04	1	11D1-04 D20 CRC GENERATT/CHECK
4864800 K	WD03	1	11D1-03 D20 RDDR MARK CONV.
4864405 U	WD01	1	11D1-01 D20 SER/PARRAL CONV.
4855824 A	VR20	1	79L05 TO92 VOLTAG.REG -5V
4861057 Z	UWEE	1	96502 D16 2 MONOST MULTIV VD
4865300 L	NTV2	1	74S00 D14 4 NAND 2I NO-ST
4865267 N	NTC5	1	74S04 D14 1 AND-OR NO-ST
4865025 P	NSD2	1	74S86 D14 4 EXOR 2I
4865304 J	NEV1	1	74S04 D14 6 INVER
4865268 B	WEH2	3	7438 D14 4 NAND 2I BUF OC
4866287 C	NDD2	1	74L32 D14 4 OR 2I
4865271 E	NSC3	1	74S11 D14 1 AND-OR INV 2 3I
4866294 Z	NSB2	1	74S02 D14 4 NOR 2I
4866315 P	NLT1	1	74L14 D14 6 INVER S-TRIG
4866312 S	NMC9	1	74L54 D14 2 IN AND-OR-INV
4866269 K	NFB2	1	74L38 D14 4 AND 2I
4866306 E	WES1	1	7404 D14 6 BUFF. HV OC
4870713 Z	MES3	2	2141H D18 RAM 1024x4 ST 70NS
4863470 Y	LRPB	1	26LS32 D16 4 LINE REC. DIFFER
4863466 D	LOPB	1	26LS31 D16 LINE DRIV H5
4863455 Y	LDE9	1	74LS244 D20 8 BUF LINE DRIV 3S
4869222 N	KR92	3	INLIB RETE RES.T.5 7x 1 KOHM
4869239 D	KR87	1	INLIB 6 PART.R 220+330 OHM
4853823 L	KDOC	1	TPQ700D D14 4 TRANS. 2PNP+2NPN
4859412 Y	DKS5	1	74S174 D16 6 D FLIP-FLOP
4859425 N	DKN8	8	74S74 D14 2 D F-F ET NO-ST
4859429 P	DKL8	1	74LS74 D14 2 D F-F ET NO-ST
4859417 Y	DKL7	2	74LS374 D20 8 D F-F EDGE-TRI
4859411 L	DKL5	2	74LS174 D16 6 D FLIP-FLOP
4859416 Z	DKE9	1	74LS273 D20 8-BIT REGISTER
4859414 R	DKE8	1	74LS175 D16 4 D FLIP-FLOP
4870263 L	DELU	1	EP6700-13 INL14 DELAY LINE
4870252 P	DELO	1	21199 D14 DELAY LINE 1GO NS
4863233 Z	DDS3	2	74LS138 D16 1/8 BIN DEC
4862275 J	CTL8	1	74LS193 D16 4-BIT BIN U/D CONT
4862272 Y	CTE8	3	74LS191 D16 4-BIT BIN U/D CT
5775130 R	CS18	1	***** SOCKET DIL 50-900
4863810 K	CS18	1	8X300 DSO INTERPRETER SIGNET
5761020 Y	TP09	25	1 PIN CAPOCORDA OCCHIELLO C.S.
4875036 Y	UZ44	1	8.0000 MHZ QUARZO-CRIST. HC18
3437600 Z	UZ18	1	***** SUPPORTO DOPPIO ADESIVO
4875050 R	UZ1B	1	20.0000 MHZ QUARZO BC1B ORIZZ.
4984163 T	RV65	1	10 KOHM 1/2W T10 POT.CERM.VER
4984072 F	RV34	1	200 OHM 1/2W T10 POT.CERM.VER
4984124 L	RV62	1	2 KOHM 1/2W T10 POT.CERM.VER
4924070 L	R97E	3	1.00 KOHM 1/4W T. 5 N.S. P.400
4924350 F	R56E	1	2.00 KOHM 1/4W T. 5 N.S. P.400
4926058 Z	R45F	1	100. KOHM 1/4W T. 5 N.S. P.400
4902317 E	R40R	2	8.25 KOHM 1/8W T. 1 R.S. P.300
4902293 K	R35R	2	3.92 KOHM 1/8W T. 1 R.S. P.300
4902263 G	R30R	2	1.50 KOHM 1/8W T. 1 R.S. P.300
4902260 X	R29R	2	1.30 KOHM 1/8W T. 1 R.S. P.300
4925058 M	R21F	2	10.0 KOHM 1/4W T. 5 N.S. P.400
4925450 M	R13J	2	27.0 KOHM 1/4W T. 5 N.S. P.600
4924698 Y	R10F	2	4.70 KOHM 1/4W T. 5 N.S. P.400
4923870 P	R90E	1	680. OHM 1/4W T. 5 N.S. P.400
4923538 T	R85E	4	330 OHM 1/4W T. 5 N.S. P.400
4923430 S	R82E	1	240 OHM 1/4W T. 5 N.S. P.400
4923073 G	R73E	4	100 OHM 1/4W T. 5 N.S. P.400
4923190 E	R43E	1	560. OHM 1/4W T. 5 N.S. P.400
4902230 U	R42R	2	511. OHM 1/8W T. 1 R.S. P.300
4923312 T	R32F	1	200. OHM 1/4W T. 5 N.S. P.400
4923431 T	R0B3	1	270. OHM 1/4W T. 5 N.S. P.600
4923231 P	R07F	1	150 OHM 1/4W T. 5 N.S. P.400
4932725 X	R066	2	51.0 OHM 1/4W T. 5 N.S. P.600
4848551 M	Q128	1	2N2907 TO18 PNP 600MA 40V
4849700 T	Q129	1	2N5320 TO39 NPN 2 A 75V SI
4849690 W	Q114	1	2N3904 TO92 NPN 200MA 40V SI
5775021 Y	PDWR	3	D1L20 SOCKET PASSO 300
5091810 S	L042	1	4.70 MH TIO INDUT.A.F.SI-SC
5091554 D	L040	1	3.30 MH TIO INDUT.A.F.SI SC
5785980 G	J086	2	M. 900- 4 VIE AMP-MODU I CC
5785920 S	J319	4	M. DIR. 3 VIE MINIVIP PIDO
5785930 T	J318	7	M. DIR. 2 VIE MINIVIP PIDO
	J141	1	PATTERN 10X2 PAS BY 100 MILS
	J139	1	PATTERN 25X2 PAS BY 100 MILS
	J138	1	PATTERN 17X2 PAS BY 100 MILS
4882009 P	D186	1	MV1404 12V .5A DIODO TUNING
4800152 S	D166	2	1N4148 75V 0.3A DIODO SEG.SI
5775023 G	LTB2	1	***** SOCKET DIL 24-600
4863498 M	LTB2	1	8T31 D24 8-BIT BIDIREC PORT
5056301 C	C522	1	22.00 MF 50V T-10+ 50 ALL.
5070709 A	C450	57	0.10 MF 50V T-20 +80 CER.
5037454 E	C203	3	10.00 MF 25V T-10 +50 ALL.
5070565 X	C666	2	68 PF 50V T+5-5 CE.A5
5070655 Y	C658	1	6800 PF 50V T-20 +20 CER.
5070577 J	C657	1	330 PF 50V T-20 +20 CER.
5070578 Y	C656	1	150 PF 50V T-20 +20 CER.
5070556 A	C654	1	47 PF 50V T-20 +20 CER.
5070542 G	C653	1	22 PF 50V T-20 +20 CER.
5070600 D	C611	1	390 PF 30V CER.A

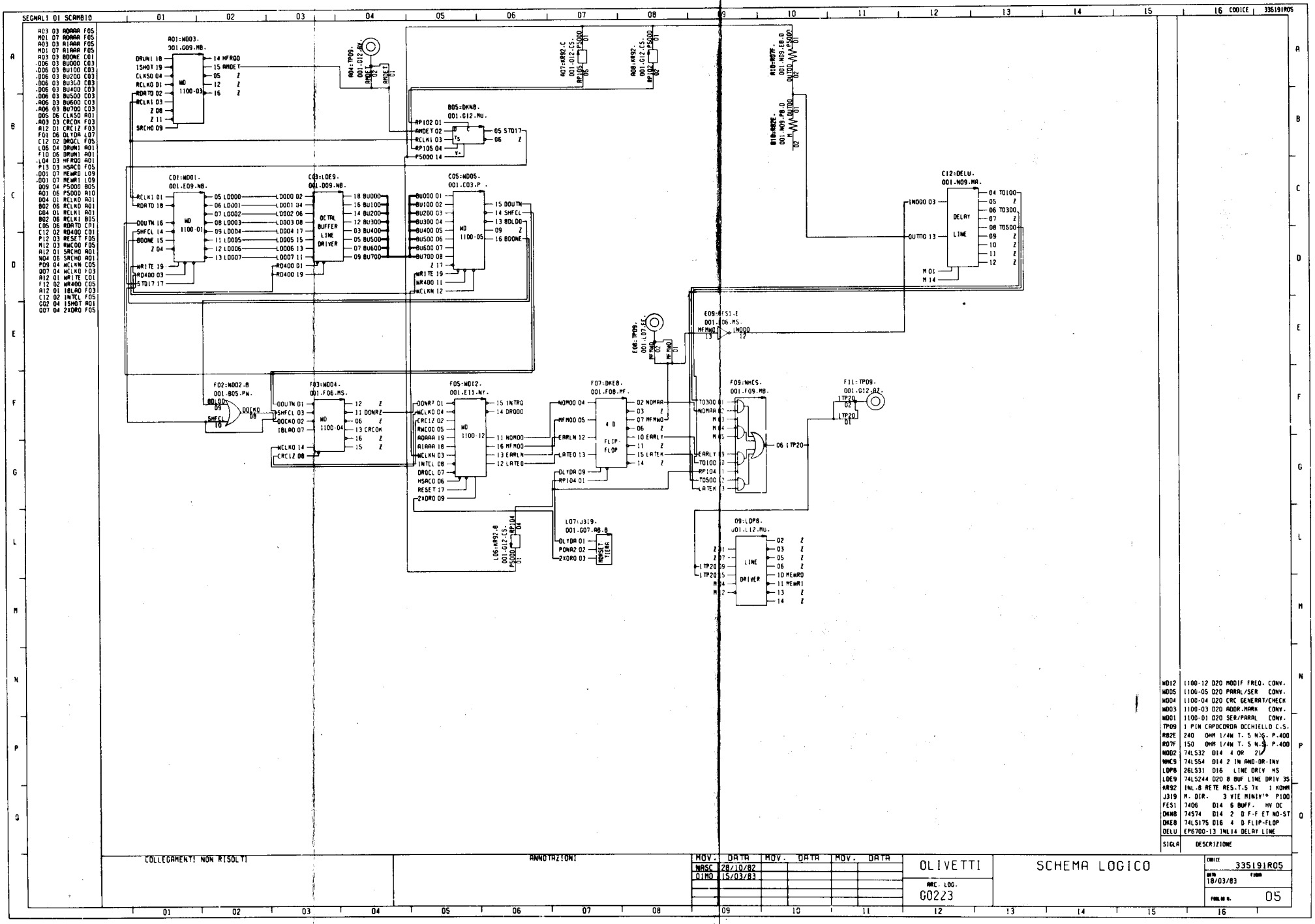
OLIVETTI	COMPLESSIVO VIMO PIASTRA 001 G0223			N. DISEGNO	335191R
ARCHIVIO LOGICO G0223	PER XP1000	MOV.	DATA	MOV.	DATA
SOSTITUISCE IL		INCR	28/10/82		
SOSTITUITO DA		NASC	20/01/83	NPM	
		OIMO	15/03/83		
		O2MO	20/05/83	DATA	30/05/83
				SCALA	1:1
				CODICE	335191R











SIGLA	DESCRIZIONE
WD12	1100-12 D20 MODIF FREQ. CONV.
WD05	1106-05 D20 PARAL/SER CONV.
WD04	1100-04 D20 CRC GENERAT/CHECK
WD03	1100-03 D20 ADDR.MARK CONV.
WD01	1100-01 D20 SER/PARAL CONV.
TP09	1 PIN CAPOCORDA OCCHIELLO C.S.
RB2E	240 OHM 1/4W T. 5 N.S. P.400
RD7F	150 OHM 1/4W T. 5 N.S. P.400
NAD2	74LS32 D14 4 OR 2I
NAC9	74LS54 D14 2 IN AND-OR-INV
LDP8	26LS31 D16 LINE DRIV MS
LDE9	74LS244 D20 8 BUF LINE DRIV 3S
KR92	INL.8 RETE RES.T.5 7x 1 KOHM
J319	M. DIR. 3 VIE MINIY'° P100
FES1	7406 D14 6 BUFF. HV OC
DKN8	74S74 D14 2 D F-F ET NO-ST
DKE8	74LS175 D16 4 D FLIP-FLOP
DELU	EP6700-13 INL14 DELAY LINE

COLLEGAMENTI NON RISOLTI

ANNOTAZIONI

MOV.	DATA	MOV.	DATA	MOV.	DATA
MASC	28/10/82				
OIMO	15/03/83				

OLIVETTI

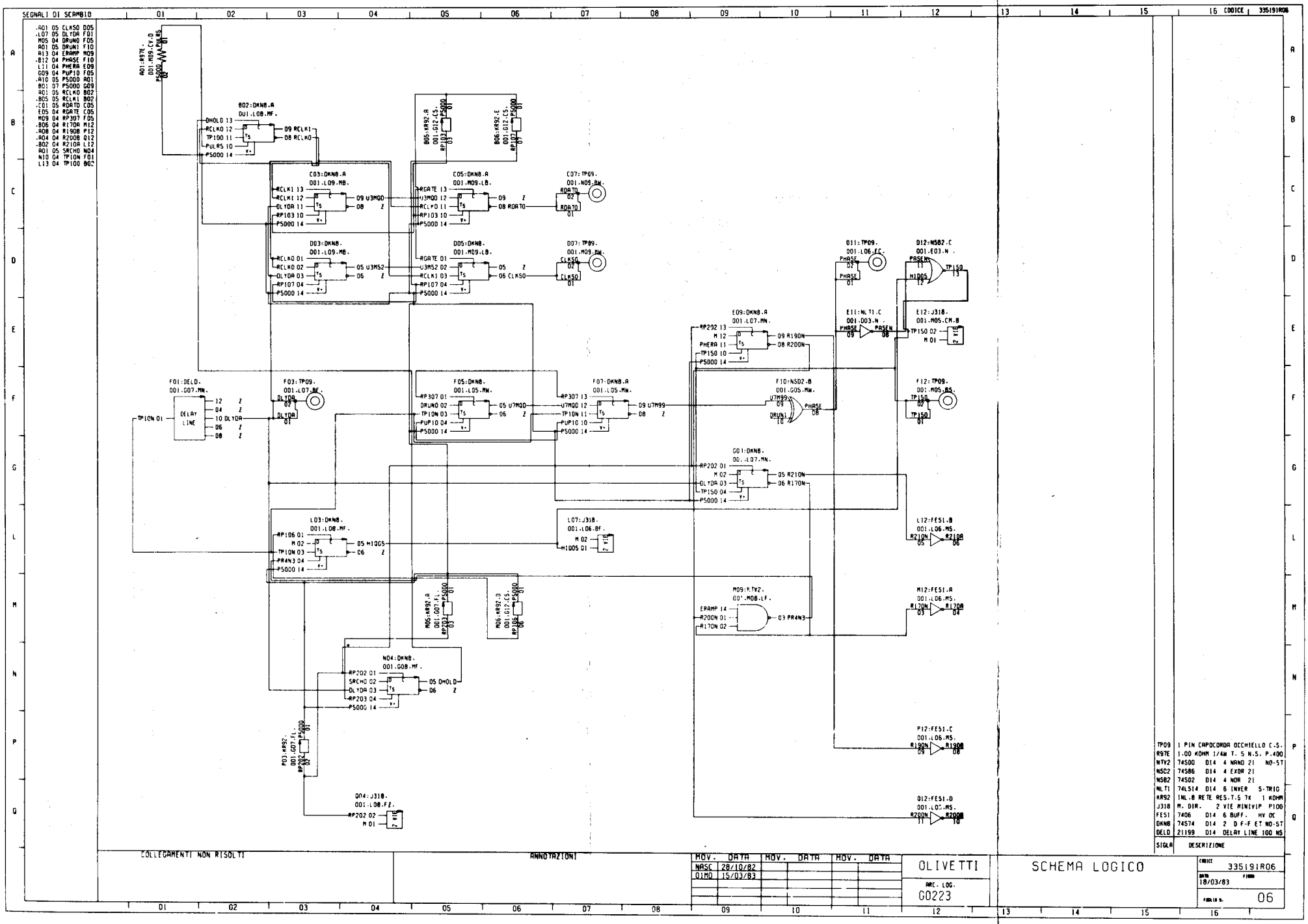
ARC. LOG. G0223

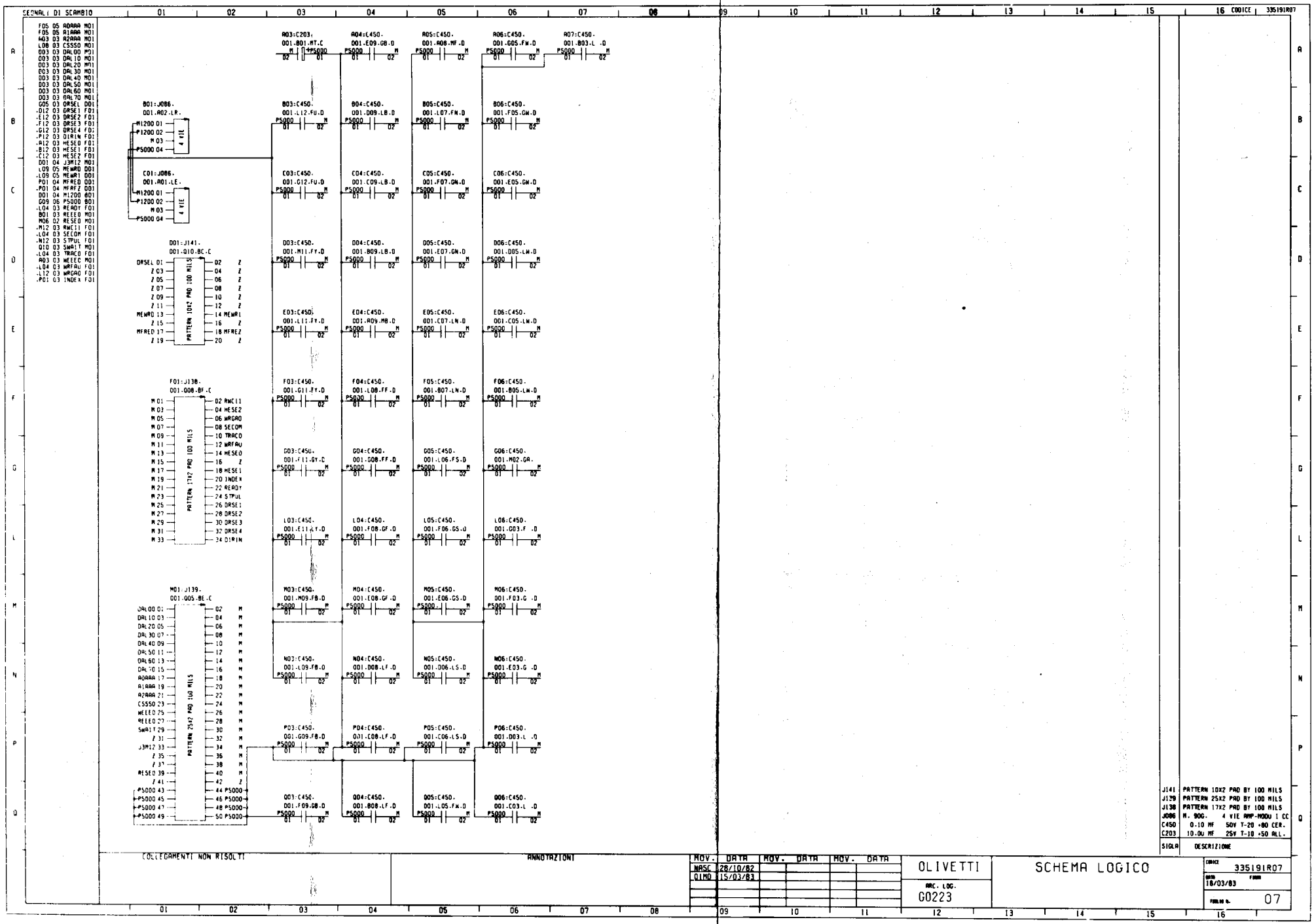
SCHEMA LOGICO

CODICE 335191R05

DATA 18/03/83

FOGLIO n. 05

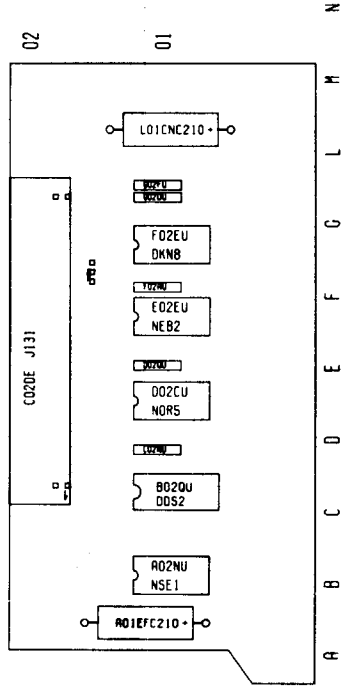




CO2NU-C450
DO2GU-C450
FO2AU-C450
FO2BM-J319
GO2DU-R97E
GO2FU-R97E
AO1 -J356

CODICE
335592K

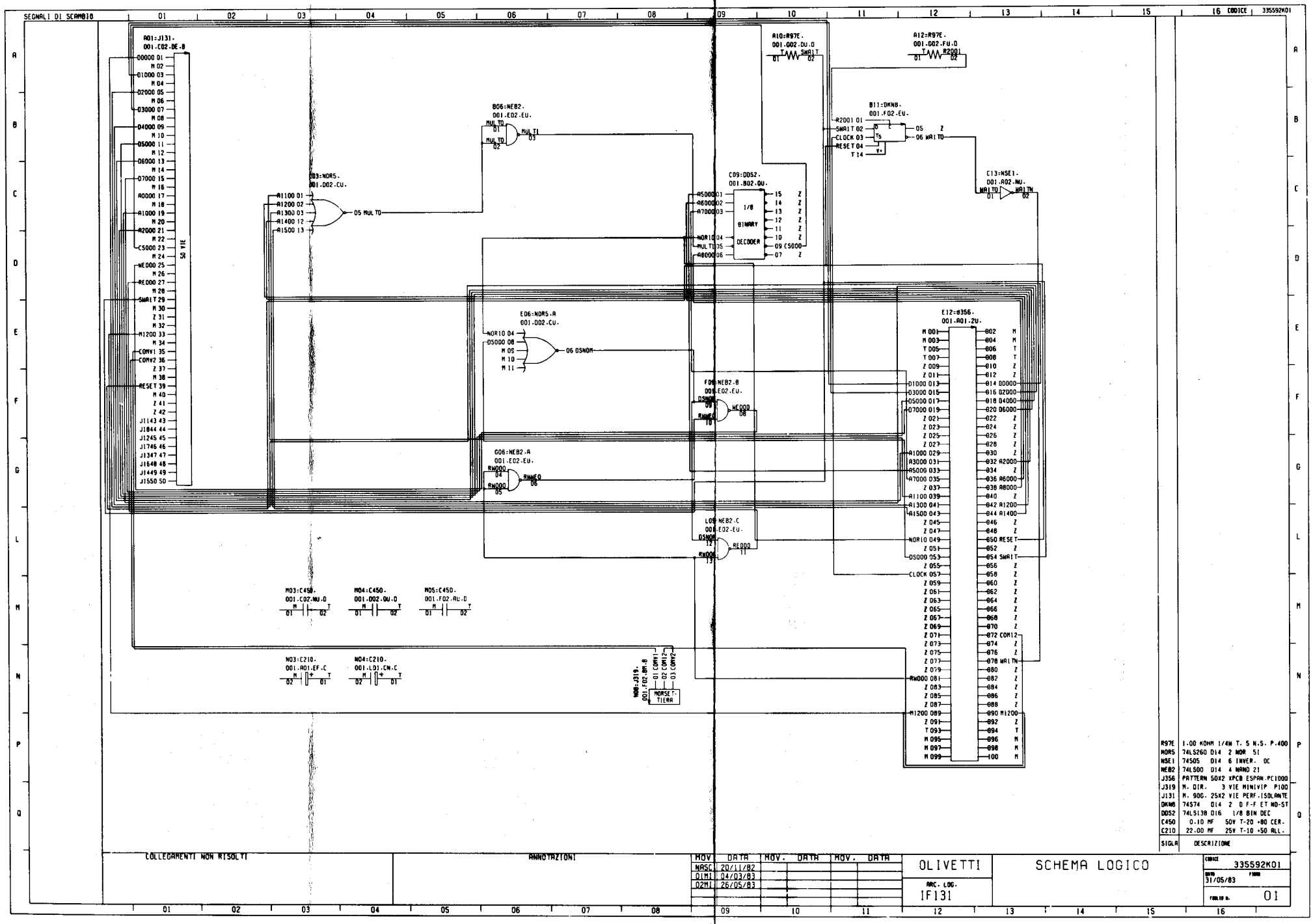
335592K06		SCHEMA PONTICELLATURE
335592K01		SCHEMA LOGICO
335592K02		STIP
335592K03		STAR
335592K04		CAPO

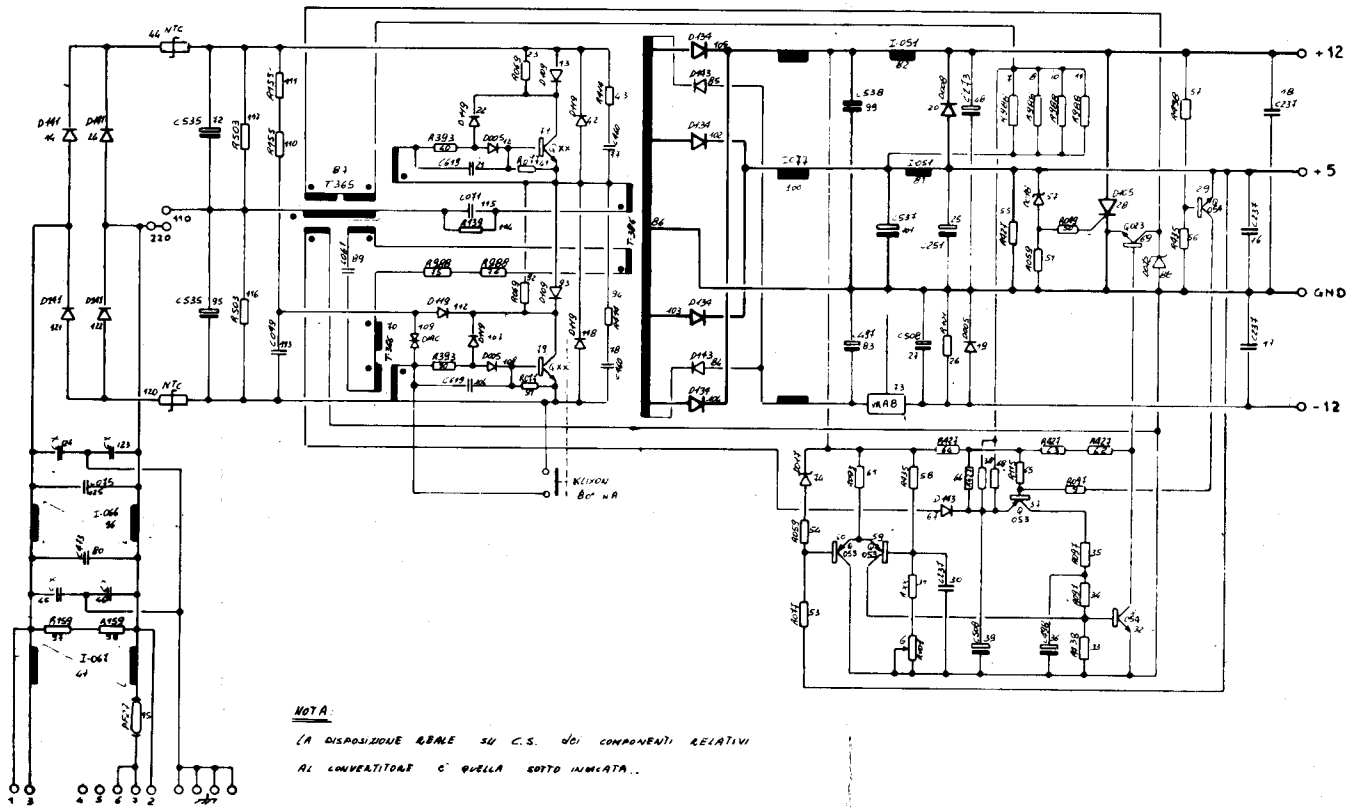


CODICE	RIF.	Q.TA	DESCRIZIONE
167003 Y	ZTAR	0001	TARGHETTA DATI PIASTRA
339117 S		0001	CIRCUITO STAMPATO
4866263 Z	NSE1	1	74S05 D14 6 INVER. OC
4866298 S	NOR5	1	74LS260 D14 2 NOR 5I
4866280 S	NEB2	1	74LS00 D14 4 NAND 2I
4859425 N	DKN8	1	74S74 D14 2 D F-F ET NO-ST
4864239 G	DDS2	1	74LS138 D16 1/8 BIN DEC
4924070 L	R97E	2	1.00 KOHM 1/4W T. 5 N.S. P.400
5787294 Q	J131	1	M. 90G. 25X2 VIE PERF.ISOLANTE
5785920 S	J319	1	M. DIR. 3 VIE MINIVIP P100
	J356	1	PATTERN 50X2 XPCB ESPAN.PC1000
5070709 A	C450	3	0.10 MF 50V T-20 +80 CER.
5053607 W	C210	2	22.00 MF 25V T-10 +50 ALL.

OLIVETTI	COMPLESSIVO VIMO PIASTRA	001 IF131	N. DISEGNO 335592K
ARCHIVIO LOGICO IF131	PER XP1000		
SOSTITUISCE IL			NPM
SOSTITUITO DA			DATA 31/05/83
			SCALA 1:1
			CODICE 335592K

MOV.	DATA	MOV.	DATA
INCR	20/11/82		
NASC	02/03/83		
DIMI	04/03/83		
02MI	26/05/83		



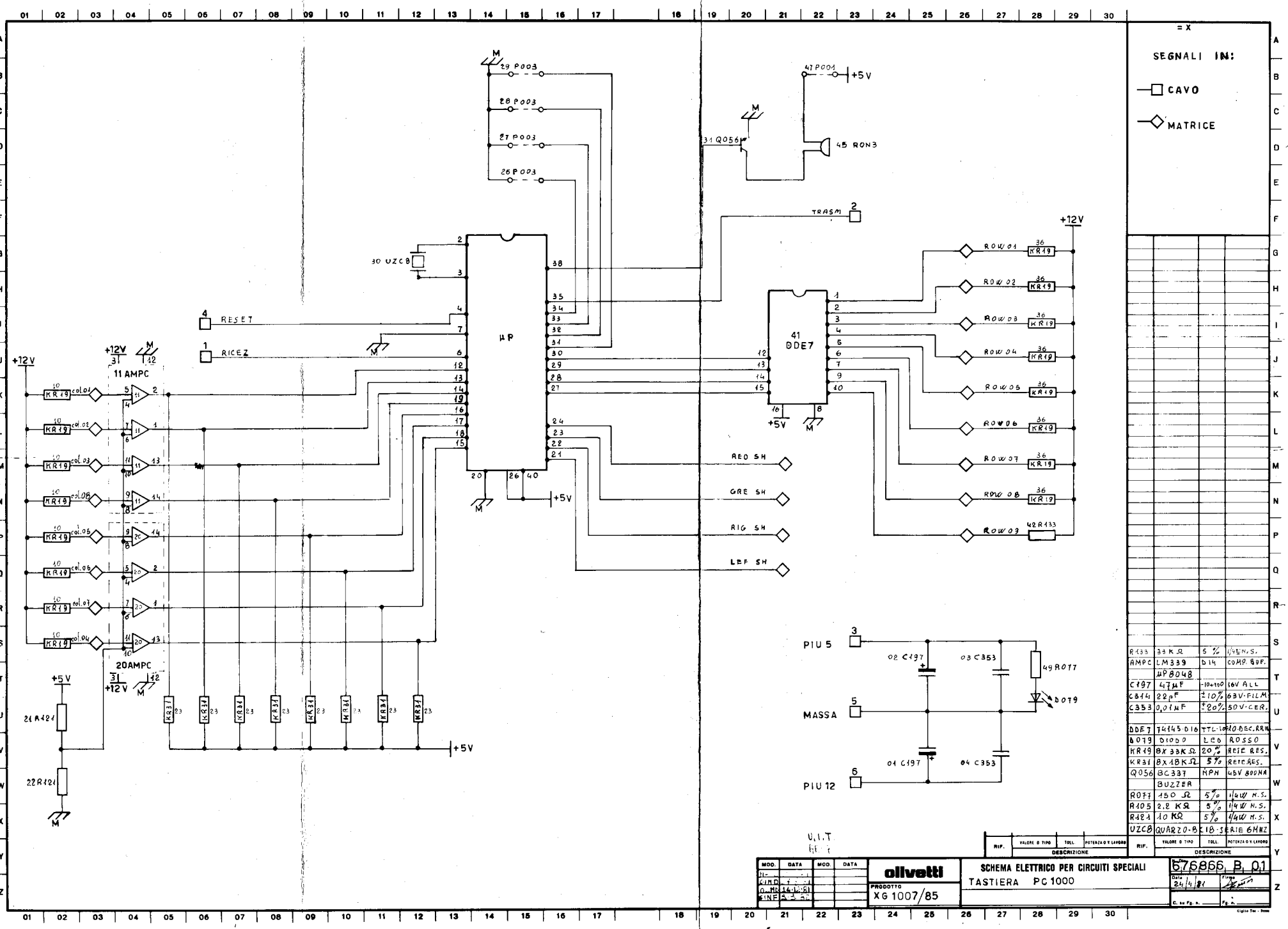


KLIXON	KLIXON 80° NORM.	AMBRA	
T 386	Trasformatore		T 386
T 366	"		T 366
T 365	"		T 365
I 067	Induttanza		I 067
I 066	"		I 066
I 077	"		I 077
I 051	"		I 051
J 064	Conn. modu I 4+4	8 vie	sfalsato
J 061	" " "	4 vie	"
VRAB	Regolatore Tensione	-12V	1A
DIAC	diac BR 100		36V 2A
NTC	Termistore NTC	20%	15 Ω
PF27	Fusibile 3,15 A		250V Rit. BPR 6,3x32
C619	Cond. 1 μF 63V		Film
G xx	Transistor 6A 60V		BUV 47
G054	" NPN 100mA		45V BC237/B
G053	" PNP "		" BC307/B
G023	" NPN 9A 60V		D44C8
R155	Res. 270 KΩ	1/4W	5%
D443	diodo 100V 1A		IN4934
D441	" 600V 3A		MR506
D434	" 100V 12A		BYW 30/100
D119	" Rapido 1A		600V IN4937
D409	" 100V 3A		MABS1
D105	Tiristore Innesc.		200V 8A
D072	diodo Zener		15V 5W
D018	" "		5,6V 0,4W
D017	" "		5,1V 0,4W
D008	" 100V 3A		IN5401
D005	" 100V 1A		IN4002
RMx	Resist. 240 Ω	5%	1/2W
C3	Condensatore		330pF 630V Scat
C538	"	±20%	4700 μF 16V
C537	"		6800 μF 10V
C535	"		470 μF 200V All
C508	"		100 μF 25V "
C498	"		470 μF 16V "
C491	"		330 μF 25V "
C473	"		0,47 μF 250V Film
C460	"		470 pF 630V poliest
C273	"		1000 μF 16V All
C251	"		2200 μF 6,3V All
C237	"		1 μF 50V Ceram.
C175	"		0,1 μF 250V Film
C071	"		6,8 μF 63V "
C061	"		1 μF 63V "
C49	"		0,1 μF 63V Film
AV01	Potenz. Filo	10%	100 Ω 1W
R88H	R. sistenza	5%	15 Ω 2W
R503	"	2%	150 KΩ 1/2W
R083	"	5%	270 Ω 1/2W
R438	"	2%	300 Ω 1/2W
R435	"	"	220 Ω "
R427	"	"	100 Ω "
R414	"	"	30 Ω "
R393	"	"	3,9 Ω "
R159	"	5%	390 KΩ 1/4W
R139	"	"	56 KΩ "
R115	"	"	56 KΩ "
R101	"	"	15 KΩ "
R091	"	"	1 KΩ "
R093	"	"	680 Ω "
R077	"	"	150 Ω "
R069	"	"	68 Ω "
R059	"	"	27 Ω "
R049	"	"	10 Ω "
Rif.	VALORE e TIPO	TOLL.	POTENZA e V. LAVORO

DESCRIZIONE

Cod. Finito 126775 Y B1

* Per stab. Esteri	Le tolleranze sono espresse in micron (μm)		Fori senza toll. ± B13
olivetti	Descrizione LA12	SCHEMA ELETTRICO	T. P. / Ar. Gest. 4 / N. Disegno
Prodotto XP1000	Materiale	Mov. Data / Mov. Data: NASC 30.9.81 / 03MD 18.6.83; ACS 30.10.81; 01MD 23.11.81; 02MD 23.12.81; 03MD 24-2-82; 04MD 11-5-82	Firma / Visto / Data 30-9-81 / Scala 2 / Cod. Brisch / Cod. Semilav. / Cod. Greggio / Cod. Finito 126775 Y-B1
Sostituisce il	Tratt. Term.		
Sostituito da	Finitura		
Derivato da			



R133	33 KΩ	5 %	1/4W N.S.
AMPC	LM339	D14	COMP. BDF.
	μP8048		
C197	47 μF	-10+100	16V ALL
C314	22 pF	±10%	63V-FILM
C353	0,01 μF	±20%	50V-CER.
DDE7	74145-D16	TTL-1	10-DEC.RRU
D079	DIODO	LED	ROSSO
KR19	8X 33KΩ	20%	RETE RES.
KR31	8X 4,8KΩ	5%	RETE RES.
Q056	BC337	NPN	45V 800MA
	BUZZER		
R077	150 Ω	5%	1/4W N.S.
R105	2,2 KΩ	5%	1/4W N.S.
R121	10 KΩ	5%	1/4W N.S.
UZC8	QUARZO-B	C18-S	SERIE 6MHZ

RIF.	VALORE O TIPO	TOLL.	POTENZA O V. LAVORO	DESCRIZIONE

MOD.	DATA	MOD.	DATA
DI-	- -		
DIMO	7 - 81		
DI-MO	16/12/81		
DINF	2 - 82		

olivetti

PRODOTTO XG 1007/85

SCHEMA ELETTRICO PER CIRCUITI SPECIALI

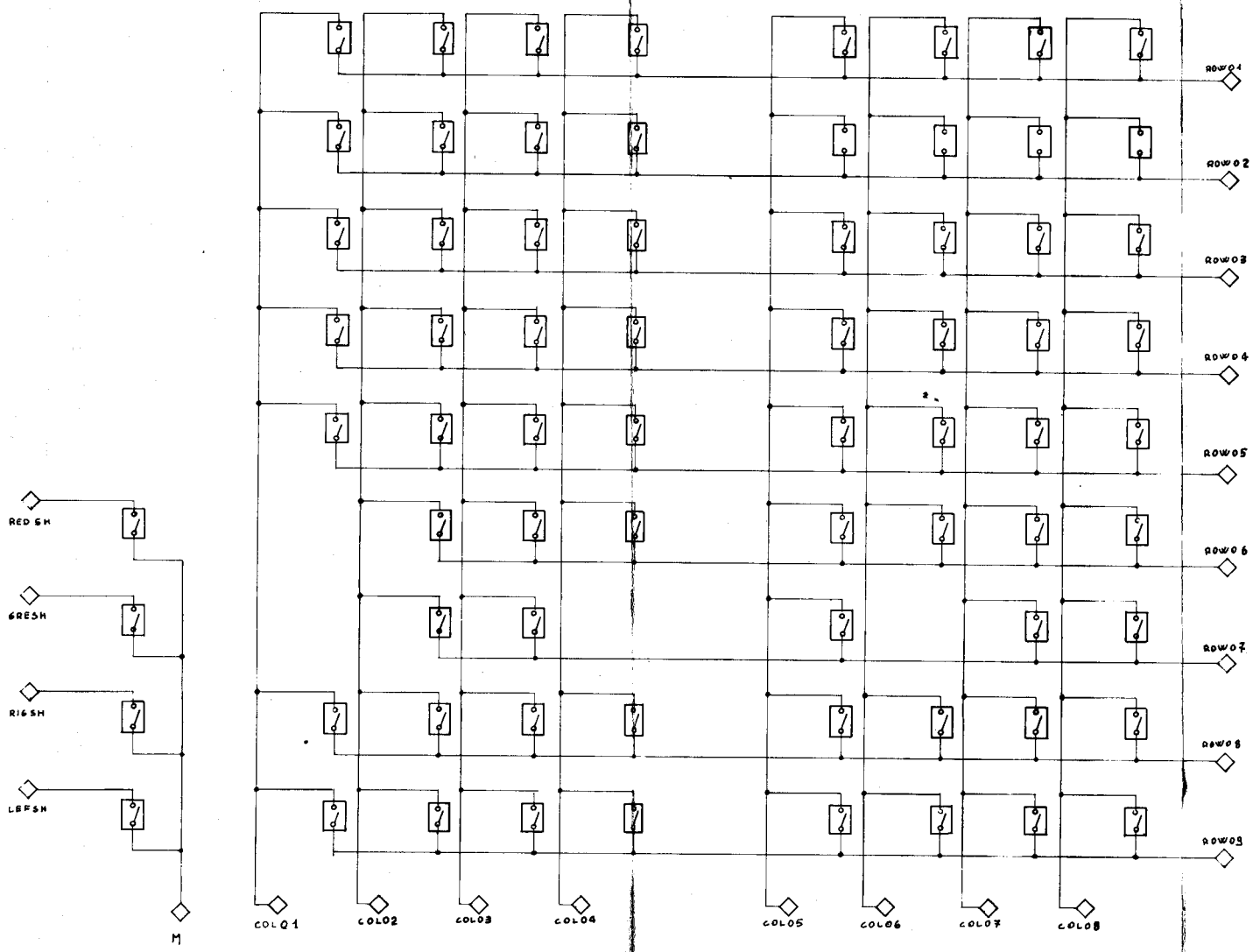
TASTIERA PC 1000

Codice 676866 B 01

Data 24/4/81

Firma

C. su Fg. n. — Fg. n.



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RIF.	VALORE O TIPO	TOLL.	POTENZA O N. LAVORO	DESCRIZIONE

MOD.	DATA	MOD.	DATA
Nr. 6			
SINP			

olivetti

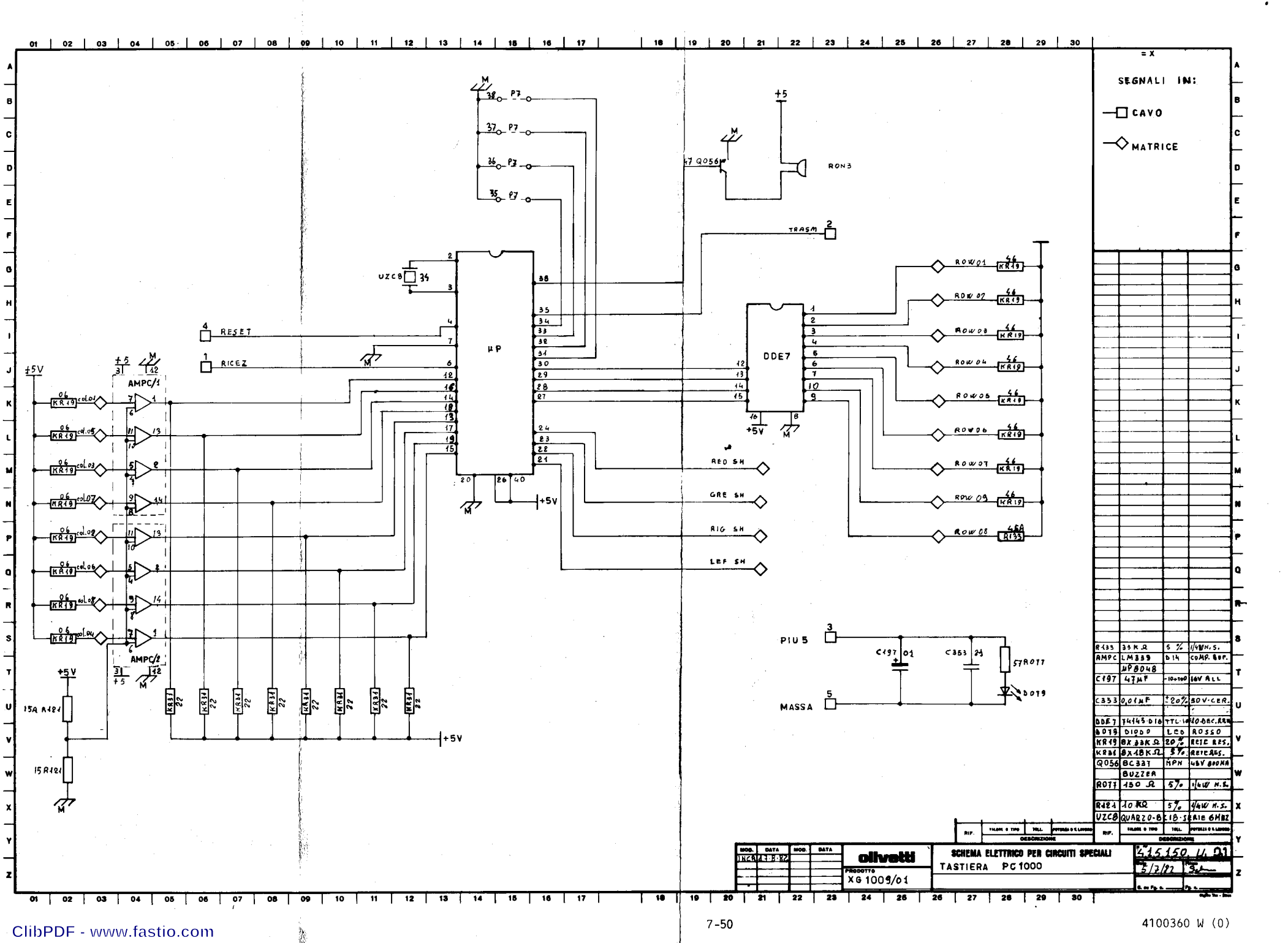
PRODOTTO X64007/85

SCHEMA ELETTRICO PER CIRCUITI SPECIALI
ELETRICAL D.W.G.
TASTIERA PC1000

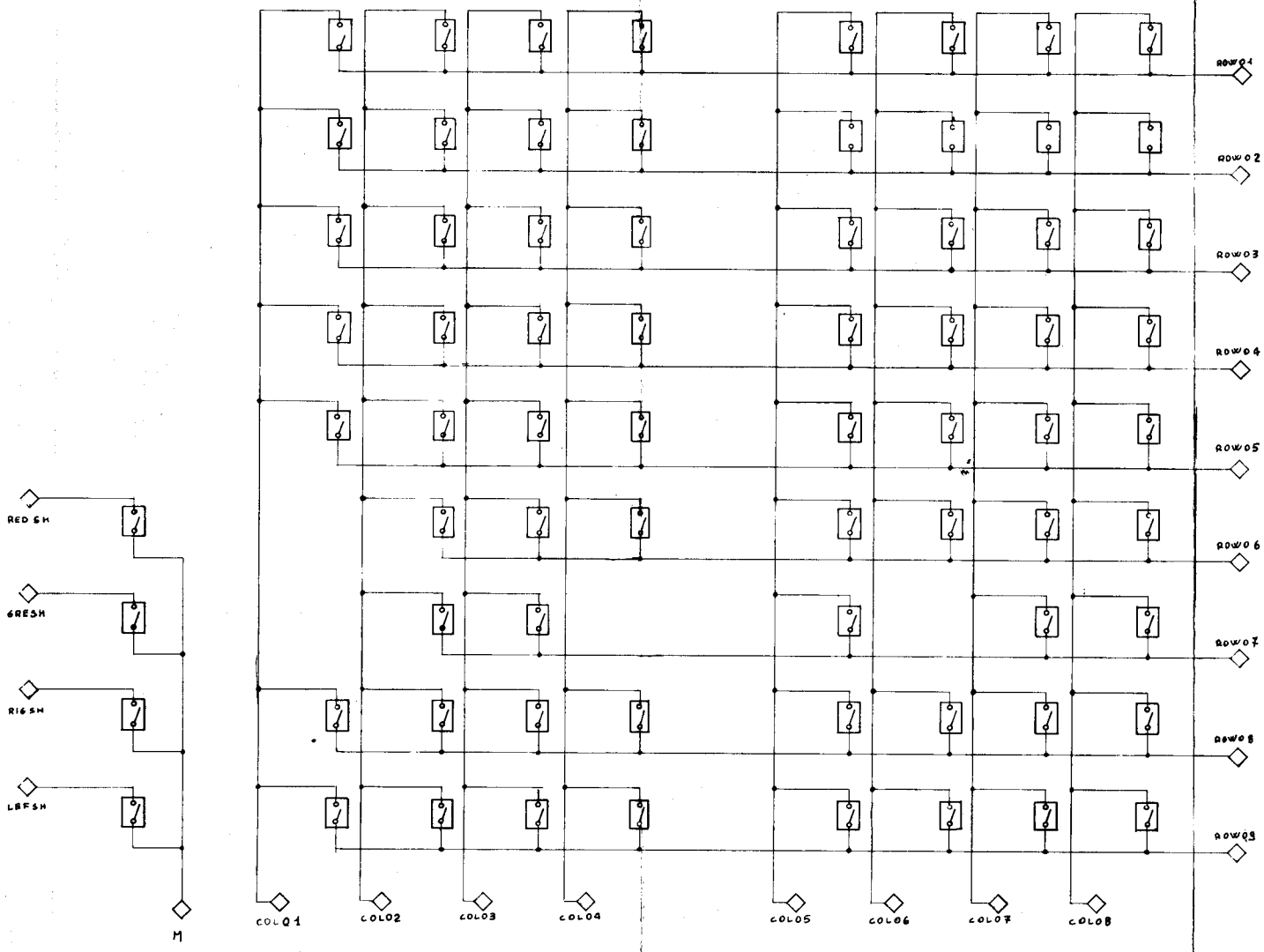
N. Dis. 6176866B 02

Data | Firma

C. as Fg. n. | Fg. n.



R435	33 KΩ	5 %	1/4W N.S.
AMPC	LM339	D14	COMP. 6OP.
	μP8048		
C197	47 μF	-10+100	16V ALL
C353	0,01 μF	±20%	50V CER.
DDE7	74145 D16	TTL	10 DEC. ARR.
D079	DIODO	LED	ROSSO
KR19	8X 33K Ω	20%	RETE RES.
KR36	8X 18K Ω	5%	RETE RES.
Q056	BC337	NPN	45V 800MA
	BUZZER		
ROTT	150 Ω	5%	1/4W N.S.
R424	10 KΩ	5%	1/4W N.S.
UZC8	QUARZO-BASE 8-SERIE 6MHZ		



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MOD.	DATA	MOD.	DATA
INCA	11-8-82		

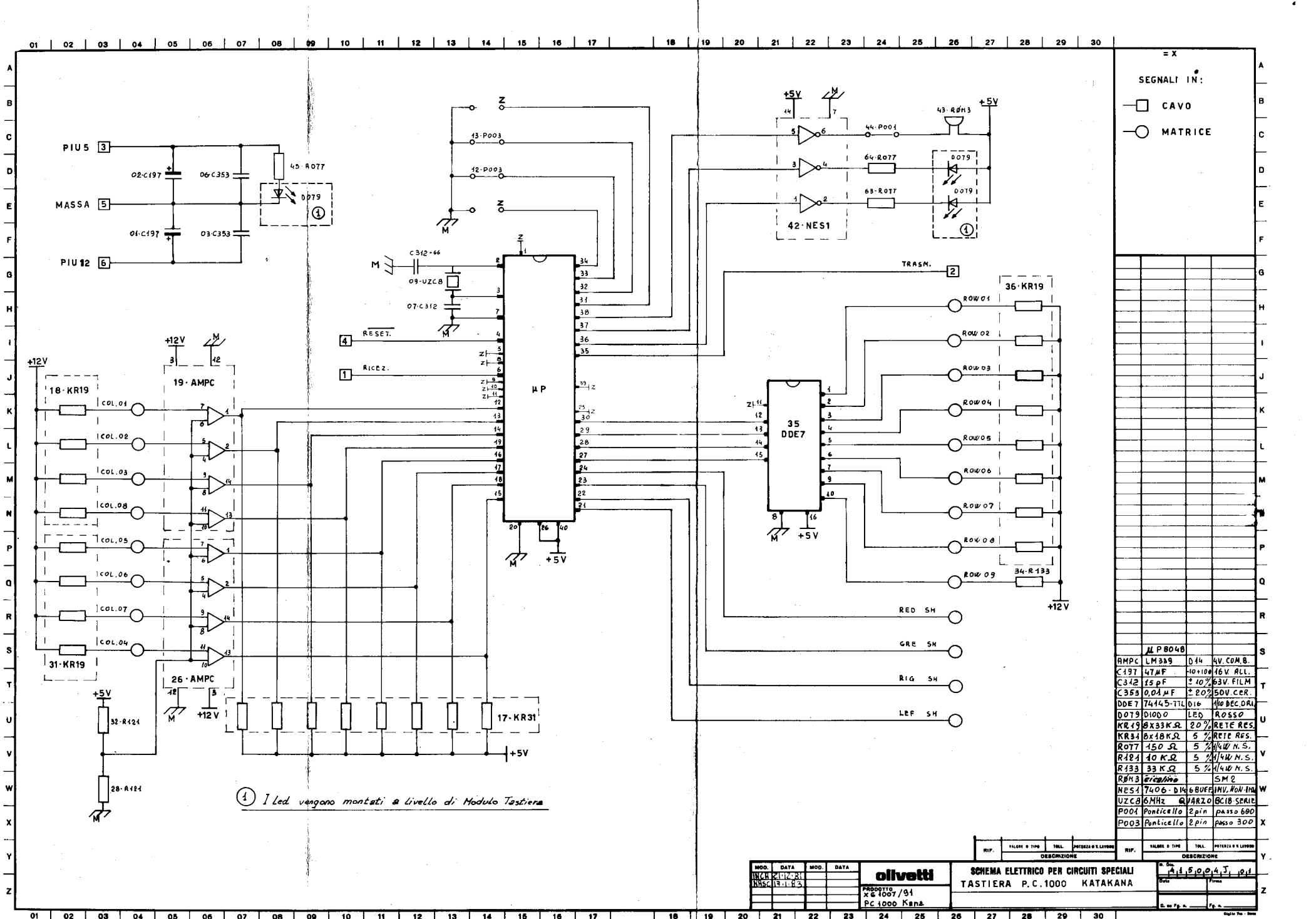
olivetti

PRODOTTO X61009/01

SCHEMA ELETTRICO PER CIRCUITI SPECIALI
ELETRICAL D.W.G.
TASTIERA PC1000

N. Dis. 4151504 02
Data 5/7/82
Pag. 32

RIF.	VALORE O TIPO	TOLL.	POTENZA O 'K LAVORO	DESCRIZIONE



	µP8048		
AMPC	LM339	D14	4V. COM.B.
C197	47µF	-10+100	16V. ALL.
C312	15 pF	± 10%	63V. FILM
C353	0,01 µF	± 20%	50V. CER.
DDE7	74145-TTL	D16	1/10 DEC. DRI.
D079	D1000	LED	ROSSO
KR19	8x33KΩ	20%	RETE RES.
KR31	8x18KΩ	5 %	RETE RES.
R077	150 Ω	5 %	1/4W N.S.
R124	10 KΩ	5 %	1/4W N.S.
R133	33 KΩ	5 %	1/4W N.S.
RØM3	eriginino		SM2
NES4	7406 - D14	6 BUFF.	INV. NON INV.
UZC8	6MHz	QUARZO	8C18 SERIE
P004	Ponticello	2 pin	passo 600
P003	Ponticello	2 pin	passo 300

RIF.	VALORE O TIPO	TOLL.	POTENZA O V. LAVORO	DESCRIZIONE

MOD.	DATA	MOD.	DATA
INCH	21-12-83		
ANSC	13-1-84		

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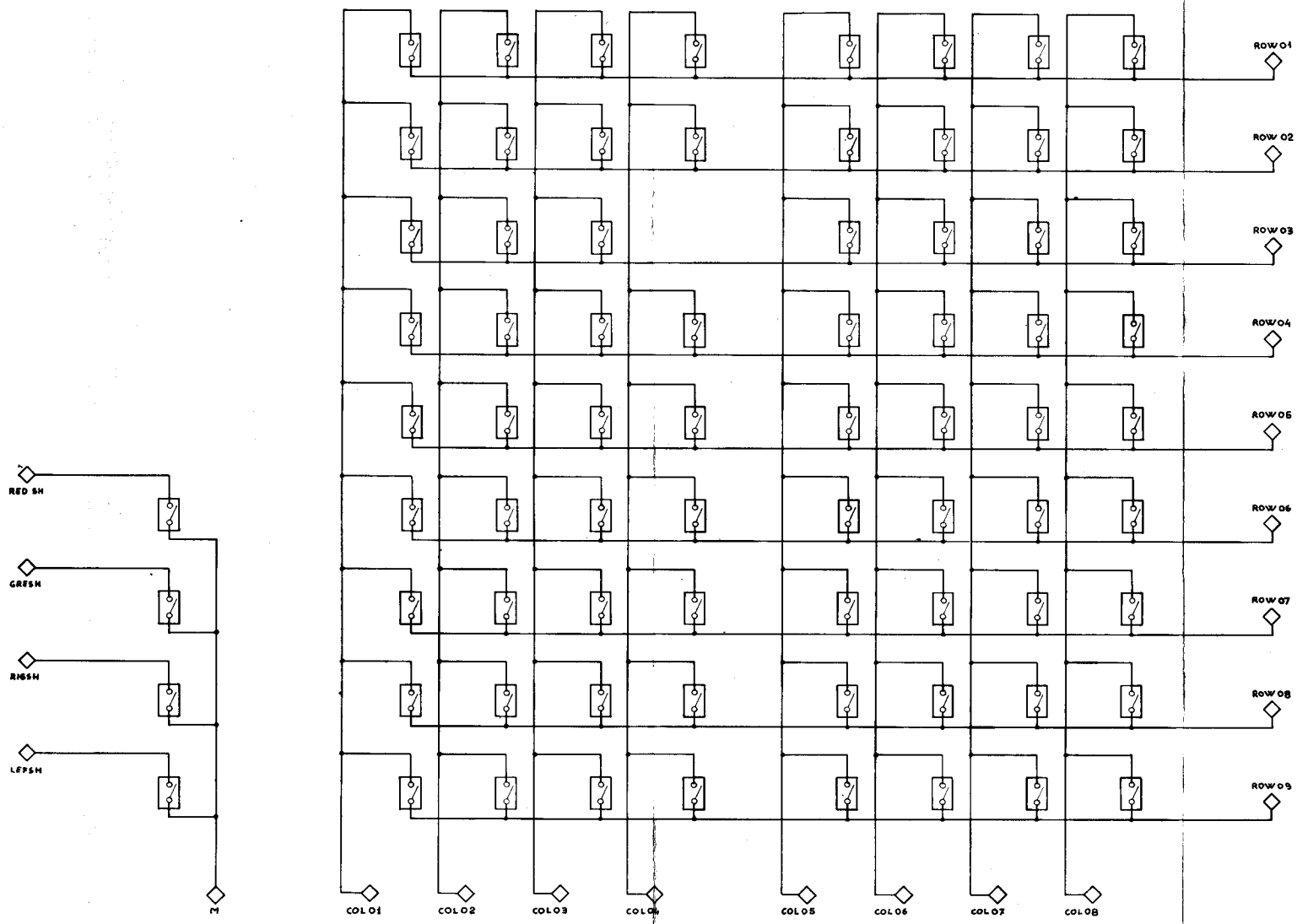
PRODOTTO
XG 1007/91
PC 1000 Kana

SCHEMA ELETTRICO PER CIRCUITI SPECIALI
TASTIERA P.C.1000 KATAKANA

N. Dis. 4 1 5 0 0 4 J 0 1

Data | Firma

D. su Fg. n. | Fg. n.



= X

MOD.	DATA	MOD.	DATA
INCR	1.12.81		
ROSE	13.1.83		

olivetti

PRODOTTO XC 4003 / 91
PC 1000 Kana

SCHEMA ELETTRICO PER CIRCUITI SPECIALI
Elettrical D.W.G.

Tastiera PC1000 Kana

N. Dis. 141504 J 02

Data | Firma

A. UNDERSTANDING THE LOGIC DIAGRAMS

CONTENTS

A. UNDERSTANDING THE LOGIC DIAGRAMS

A.1 GENERAL

The form of the logic diagrams included in this manual are specific to Olivetti. The following is included to assist in the understanding of the logic diagrams.

A.2 LOGIC DIAGRAM REFERENCING

The logic symbol used for a particular logic element is consistent throughout the diagrams. The referencing associated with these elements is shown in Figure A-1

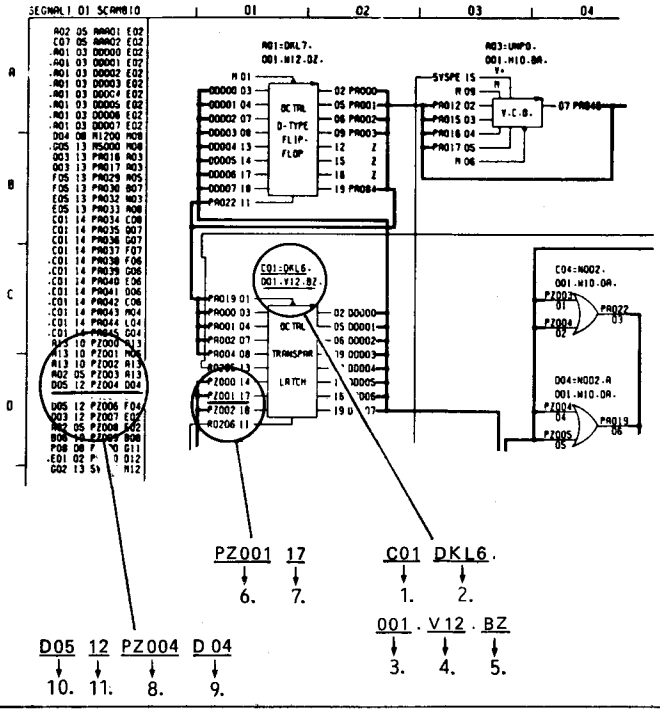


Fig. A-1 Logic Diagram Referencing

1. Coordinates giving the position of the logic symbol on the logic diagram.

2. Component code - A description of the code giving component type and function is found in the lower right hand corner of the logic diagram.

3. Board Number - For the M20 this is always 001 as no logic circuit is divided between several printed circuit boards.

4. Coordinates giving physical location of the component on the printed circuit board.

5. Coordinates giving the position of the logic element within the component or its position within a component location.

6. Signal Name

7. Component Pin Number

8. Signal name of a signal path that covers more than one logic diagram.

9. Coordinates giving the location of the signal this logic diagram.

10 & 11. Coordinates giving the location of the signal on other logic diagrams and the relevant logic diagram sheet number.

A.3 LOGIC DIAGRAM SIGNAL NAMES

The following relates the Mnemonics used in the text of this manual to the Signal Names used on the logic diagrams.

Mnemonic	Signal Name
A0	AAA00
A1	AAA01
A2	AAA02
A3	AAA03
A4	AAA04
A5	AAA05
A6	AAA06
A7	AAA07
A8	AAA08
A9	AAA09
A10	AAA10
A11	AAA11
A12	AAA12
A13	AAA13
A14	AAA14
A15	AAA15
*ACK/PC6	R0610
AD0	PL000
AD1	PL001
AD2	PL002
AD3	PL003

Mnemonic	Signal Name
AD4	PL004
AD5	PL005
AD6	PL006
AD7	PL007
AD8	PL008
AD9	PL009
AD10	PL010
AD11	PL011
AD12	PL012
AD13	PL013
AD14	PL014
AD15	PL015
AS	PZ121
*AS	PL022
*AS	PZ122
BCLK	PZ127
BLUE	PF009
BOOT	PZ015
*BOOT	R0904
BUSACK	PZ120
*BUSACK	R0406
*BUSACKIN	R0405
*BUSACKOUT	R0408
*BUSREQ	R1008
BUSY/PB1	R0304
B/*W	PL018
B/*W	PZ021
BW VIDEO	R0026
BW/*COLOR	PZ002
B/W RMCS0	PZ024
B/W RMCS1	PZ026
B/W RMCS2	PZ027
B/W RMCS3	PZ029
CAS0	PK044
CAS1	PK045
CAS2	PK046
CASL	PZ042
CASU	PZ043
CHAR CLOCK	PZ039
COLOR RMCS1	PZ032
COLOR RMCS2	PZ028
COLOR RMCS3	PZ031
COLOR4/*COLOR8	PZ000
*COMVI1	R0002
*COMVI2	R0004
CPU LATCH	PZ040
CPUCLK	PZ018
*CPU/CRT	PB033
CPU/*CRT	PZ038
CRT LATCH	PZ039
CTS	PH007
CTS	PH027
D0	DDD00

Mnemonic	Signal Name
D1	DDD01
D1/PA0	R0103
D2	DDD02
D2/PA1	R0104
D3	DDD03
D3/PA2	R0105
D4	DDD04
D4/PA3	R0106
D5	DDD05
D5/PA4	R0107
D6	DDD06
D6/PA5	R0108
D7	DDD07
D7/PA6	R0109
D8	DDD08
D9	DDD09
D10	DDD10
D11	DDD11
D12	DDD12
D13	DDD13
D14	DDD14
D15	DDD15
DA8/PA7	R0110
*DCPU	PB008
*DCRT	PB009
*DDEN	PA003
DEMAND/PB2	R0305
DI0	PC024
DI1	PC025
DI2	PC026
DI3	PC027
DI4	PC028
DI5	PC029
DI6	PC030
DI7	PC031
DI8	PC032
DI9	PC033
DI10	PC034
DI11	PC035
DI12	PC036
DI13	PC037
DI14	PC038
DI15	PC039
*DIR	PA041
DIRC	PA026
DISPEN	PZ098
*DRAM	PZ013
DRAMSEL	PZ023
DS	PZ103
*DS	PL017
*DS	PZ064
DSR	PH008
DSR	PH026
DTR	PH031

Mnemonic	Signal Name
*DTR	PH011
*DTR	PH014
E	R0018
EARLY	PA008
EMPTY/PB3	R0306
FAULT/PB5	R0308
GRAPHCLK1	PZ065
GRAPHCLK2	PF026
GRAPHDB	PZ068
GRAPHDG	PZ085
GRAPHDR	PZ067
*GRAPHLD1	PZ017
*GRAPHLD2	PF024
GREEN	PF007
HLD	PA023
HLT	PA023
HSYNC	PZ096
HSYNC	R0102
*I/01	PZ006
*I/02	PZ004
*I/04	PZ094
*I/05	PZ126
*I/06	PZ108
*I/07	PZ106
*I/010	PZ114
*I/011	PZ123
*I/013	PZ099
*INDEX	PA036
INT	PK038
INTFDC	PZ009
INTPC0	PZ118
INTPC3	PZ117
INTRXDKY	PZ112
INTRXDRT	PZ110
INTTXDKY	PZ113
INTTXDRT	PZ111
*I/O RD	PZ005
I/O REQ	PZ124
*I/O WR	PZ003
*IP	PA036
IR0	PZ009
IR1	PK033
IR2	PK034
IR3	PZ110
IR4	PZ112
IR5	PK034
IR6	PK036
IR7	PK037
LATE	PA009
MA0	PE000
MA0	PE016
MA1	PE001
MA1	PE017
MA2	PE002

Mnemonic	Signal Name
MA2	PE018
MA3	PE003
MA3	PE019
MA4	PE004
MA4	PE020
MA5	PE005
MA5	PE021
MA6	PE006
MA6	PE022
MA7	PE007
MA7	PE023
MA8	PE008
MA8	PE024
MA9	PE009
MA9	PE025
MA10	PE010
MA10	PE026
MA11	PE011
MA11	PE027
*MEMDIS	R0503
*MICRO 1	R0706
*MOTOR ON	PA045
*MR	PZ008
MREQ	PZ100
*MREQ	PL020
*MREQ	PZ016
MX0	PZ055
MX1	PZ056
MX3	PZ058
MX4	PZ059
MX5	PZ060
MX6	PZ061
MX7	PZ062
MXA0	PZ047
MXA1	PZ048
MXA2	PZ049
MXA3	PZ050
MXA4	PZ051
MXA5	PZ052
MXA6	PZ053
MXA7	PZ054
MXB0	PZ086
MXB1	PZ087
MXB2	PZ088
MXB3	PZ089
MXB4	PZ090
MXB5	PZ091
MXB6	PZ092
MXB7	PZ093
*NMI	R1004
N/*S	PL019
N/*S	R0806
*NVI	PZ119
*OBMS	PZ030

Mnemonic	Signal Name
*OE	PG000
PA0	PJ000
PA0/D1	R0103
PA1	PJ001
PA1/D2	R0104
PA2	PJ002
PA2/D3	R0105
PA3	PJ003
PA3/D4	R0106
PA4	PJ004
PA4/D5	R0107
PA5	PJ005
PA5/D6	R0108
PA6	PJ006
PA6/D7	R0109
PA7	PJ007
PA7/D8	R0110
PB0	PJ008
PB0	R0303
PB1	PJ009
PB1/BUSY	R0304
PB2	PJ010
PB2/DEMAND	R0305
PB3	PJ011
PB3/EMPTY	R0306
PB4	PJ012
PB4/SELECTED	R0307
PB5	PJ013
PB5/FAULT	R0308
PB6	PJ014
PB6	R0309
PB7	PJ015
PB7	R0310
PC0	PZ118
PC0	R0603
PC1	PJ016
PC1	R0605
PC2	PJ017
PC2	R0606
PC3	PZ117
PC3	R0607
PC4	PJ018
PC4	R0608
PC5	PJ019
PC5/*STROBE	R0609
PC6	PJ020
PC6/*ACK	R0610
PC7	PJ021
PC7	R0604
*PD	PA012
PU	PA012
RA0	PE012
RA0	PE028
RA1	PE013

Mnemonic	Signal Name
SN0	PK018
SN1	PK012
SN1	PK019
SN2	PK013
SN2	PK020
SN3	PK014
SN3	PK021
SN4	PK015
SN5	PK016
SN6	PK017
SPARE	PF010
*SP/*EN	R0208
*SRAM	PZ014
*SRAM	PZ014
SS0	PA025
ST0	PK007
ST0	PK018
ST1	PK008
ST1	PK019
ST2	PK009
ST2	PK020
ST3	PK010
ST3	PK021
STEP	PA027
*STEP	PA042
*STOP	R0705
*STROBE/PC5	R0609
*SWAIT	PZ102
SYSINT	R0001
T50	PZ020
T100	PB045
T150	PB043
T200	PB044
T250	PB048
TA14	PZ095
TA15	PZ010
TR00	PA037
TRACK0	PA037
TSN0	PZ011
TSN1	PZ012
TSN2	PZ035
TXC	PH019
TXC	PZ109
TXCLKA	PH018
TXCLKB	PH002
TXD	PH009
TXD	PH023
TXD	PH029
TXRDY	PZ111
TXRDY	PZ112
VCO	PA046
VDD	PD033
*VI	RI002
*VINTACK	PK043

Mnemonic	Signal Name
VSYNC	PZ097
VSYNC	R0502
WAIT	
*WAIT	
WDIN	PA007
WDOUT	PA011
*WE	PA021
*WEL	PZ046
*WEU	PZ045
*WF/*VFOE	PA010
WG	PA006
*WPRT	PA035
WR BUF EN	PC001
*WRITE DATA	PA038
*WRITE GATE	PA039
*WRITE PROJECT	PA035
1MHZ	PZ007
2MHZ	PZ105
32K/*128K	R0205
4MHZ	PM009

DATE	UPDATED PAGES	PAGES	CODE
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